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Digital PLL for ISM applications

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Abstract

In modern transceivers, a low power PLL is a key block. It is known that with the evolution of technology, lower power and high performance circuitry is a challenging demand.

In this thesis, a low power PLL is developed in order not to exceed 2mW of total power consumption. It is composed by small area blocks which is one of the main demands.

The blocks that compose the PLL are widely abridged and the final solution is shown, showing why it is employed. The VCO block is a Current-Starved Ring Oscillator with a frequency range from 400MHz to 1.5GHz, with a 300µW to approximately 660µW power consumption. The divider is composed by six TSPC D Flip-Flop in series, forming a divide-by-64 divider. The Phase-Detector is a Dual D Flip-Flop detector with a charge pump. The PLL has less than a 2us lock time and presents a output oscillation of 1GHz, as expected. It also has a total power consumption of 1.3mW, therefore fulfilling all the specifications.

The main contributions of this thesis are that this PLL can be applied in ISM applications due to its covering frequency range and low cost 130nm CMOS technology.

Keywords: PLL, VCO, Divider, Charge Pump, Loop Filter, Low Power, Area, Transceiver

Resumo

Em transceivers modernos, uma PLL de baixa potência é um bloco chave. É sabido que com a evolução da tecnologia, circuitos de baixa potência e alta performance são uma necessidade cada vez mais desafiadora.

Nesta tese de mestrado, uma PLL de baixa potência é desenvolvida de modo a não exceder os 2mW de potência total consumida. É composta por blocos simples e ocupa uma área considerada pequena, que são as maiores premissas.

Os blocos que compõem esta PLL são explorados e a solução final é imposta e demonstrado o porquê. O bloco VCO desta PLL é um Current-Starved Ring Oscillator com uma banda de frequências de 400MHz a 1.5GHz, com um consumo de 300µW a aproximadamente 660µW. O divisor é composto por seis TSPC Flip-Flop D em série, formando assim um divisor por 64. O detetor de fase é constituído por um detetor Dual Flip-Flop D com um charge pump. Esta PLL apresenta menos de 2us de tempo de lock e uma frequência de saída de 1GHz, tal como esperado. Tem também como consumo de potência total de 1.3mW, cumprindo assim todas as especificações.

As maiores contribuições desta tese são a possibilidade de ser utilizada em aplicações ISM devido à gama de frequências que cobre e ao baixo custo da tecnologia CMOS de 130nm.

Palavras-chave: PLL, VCO, Divisor, Charge Pump, Loop Filter, Baixa Potência, Área, Transceiver

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CHAPTER 1

INTRODUCTION

Over the last two decades, the continuous shrinking in the feature size of MOSFETs has increasingly attracted the research and development of low-power radio frequency CMOS integrated circuits [12]. For mobile wireless communications, low-power operations are of crucial importance for the mobile units as the battery lifetime is limited by the power consumption and the low power consumption also helps to reduce the operating temperature resulting in more stable performance. For modern transceiver architecture, a fully integrated frequency synthesizer with low power voltage-controlled oscillators (VCO) for signal generation and low power frequency dividers is always a topic of interest in research.

The need for mobile communications computing and networking has become more important than ever. Over the last decade, various wireless standards have been developed primarily for applications over short distances. These wireless standards are intended to provide fast and low cost connections to the Internet and between the portable devices with low communication range, usually between 1 and 100 meters [12]. The standards bring up the need of network applications requiring transceivers with long battery life, being these an attractive option for applications from sensor based network systems, home automation, automotive and medical solutions to many others.

Many standards have strict rules such as low cost, low power, low data rate and short range wireless networks. Most synthesizers have not scaled down the supply voltage to reduce the power consumption of digital blocks. That power consumption of the frequency synthesizer (mainly VCO and frequency divider) can be reduced significantly by further simplifying the circuit structures, and adapting some power saving techniques to the digital blocks such as frequency dividers.

1.1 Phase-Locked Loop

Phase-Locked Loops (PLLs) are essential components in many modern electronic devices. The main concept of phase locking was proposed decades ago, but still today the demand for PLL implementation grows rapidly. The reasons for increasing popularity of PLLs are high performance, low price and the increasing evolution of the IC technologies in terms of speed and complexity.

A PLL is a circuit that must be capable of synchronizing an output signal with a reference signal in both frequency and phase. The phase error between the output signal and reference signal should be maintained at zero. If the phase error builds up, a PLL control mechanism forces the phase error to be reduced to minimum. It can be seen that the phase of the output signal is "locked" to the phase of the reference signal. This is the reason it is referred to as "phase-locked loop".

PLLs are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of a RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions. Phase noise is one of the most critical performance parameters of the frequency synthesizer. The goal to meet strict phase noise, spurious-level performance and fine frequency resolution with reasonable levels of power consumption remains a challenging task for circuit designers around the world.

1.2 Motivation

The use of PLLs for generating phase synchronous and frequency multiplied clocks are popular in applications such as communications, wireless systems, microprocessors, and disk drive electronics. Some important examples of PLL application areas are illustrated in Table 1.1:

Table 1.1: Possible PLL Applications

PLL Applications	
Clock synthesis and synchronization circuits	Clock generation for microprocessors, DSP, memory
Frequency synthesizers	Local oscillator generation for wireless transceivers
Clock and data recovery circuits	Fiber optic data transceivers, disk drive electronics, local area network transceivers, DSL transceivers, Serial link transceivers
Modulator and demodulator circuits	Non-coherent modulator/demodulator in communication systems
Phase-locked receivers	Radar, Spacecrafts

There are several figures of merit that determine PLLs' performance, among which locking time, phase noise and jitter performance, and power consumption are the most important three.

Locking time is the time it takes for PLL to produce the desired output frequency to within a certain frequency error. Jitter is a random variation of the clock edges in time domain. Phase noise is the frequency domain representation of random fluctuations in the phase of a waveform. Jitter and phase noise both represent the same phenomenon but in different domains. As the CMOS technologies evolve, clock frequencies increase. Therefore more strict noise requirements are imposed on a PLL design because clocks with shorter periods are more susceptible to random variation of clock edges. For noise sensitive applications such as wireless transceivers and high speed data processing, one of the main tasks is to minimize phase noise and jitter. It is required a special attention to both individual blocks and PLL noise performances on the system behavior.

The main focus on this thesis is the power consumption. It is required that this PLL parameter should be as low as possible. It is especially important in portable applications such as cellular phones. Minimizing the power consumption usually means sacrificing the noise and jitter performance. Therefore, the design and implementation of a high performance and low power PLL requires some knowledge and experience in circuit design, as well as of the system level design trade-offs.

The main objectives of this thesis are:

- To study PLL individual building blocks, PLL system level behavior as well as system design trade-offs.
- To optimize individual building blocks of PLL for better performance and lower power consumption in 130nm CMOS technology.

The design specification of the PLL is shown in Table 1.2:

Table 1.2: PLL Design Specifications

Input Reference Clock Frequency	16 MHz
VCO Output Frequency Range	400MHz - 1.5GHz
PLL Output Frequency	1GHz
Power Consumption	< 2 mW
Technology	UMC 130nm

1.3 Main Contributions

The subject of this thesis is focused on low power and low area implementation, therefore it can be applied to any kind of circuitry that needs a PLL that fulfills the requirements in 1.2. Also, it can be applied for ISM applications. ISM stands for Industrial, scientific and medical (ISM) and its applications (of radio frequency energy) are defined by the

ITU (International telecommunications Union) as "Operation of equipment or appliances designed to generate and use locally radio frequency energy for industrial, scientific, medical, domestic or similar purposes, excluding applications in the field of telecommunications".

1.4 Thesis Structure

The structure of this thesis consists in several chapters with important aspects. Chapter 2 introduces the Transceiver concept and many of transceiver topologies. The next Chapter, 3 introduces the types of PLLs and 5 shows the blocks that constitute a PLL. In between those two chapters, a concept of Oscillation and some kind of oscillators are also introduced in Chapter 4, as well as two other important aspects, Phase Noise and Jitter, in Section 4.4. In Chapter 6 the results of the PLL are discussed and finally, in Chapter 7 the conclusions about this thesis are made.

Chapter 2

Transceivers

In this chapter the fundamentals of frequency synthesizers, basic transceiver (transmitter and receiver) architectures, and some important front-end blocks are reviewed. First the PLL frequency synthesizer is defined and a small introduction to the concept of phase noise and its effect on the transceiver is introduced. It is started by describing the function of a PLL frequency synthesizer and how it can be applied on a transceiver. Also, advantages and disadvantages of several receiver and transmitter architectures are presented. Receivers are used to perform low-noise amplification, downconversion, and demodulation, while transmitters perform modulation, upconversion, and power amplification. Receiver and transmitter architectures can be divided into two types: heterodyne, which uses one or more IFs (intermediate frequencies), and homodyne, without IF. Nowadays research is more active concerning the receiver path, since requirements such as integrability, interference rejection, band selectivity and low power are more demanding in receivers than in transmitters [12].

Noting that even if the designed PLL for this thesis is considered as "single ended"with only one output, it will be also given emphasis to architectures with quadrature outputs due to previous conceived work on quadrature-based VCO and PLL.

2.1 Use of PLL in Transceivers

A frequency synthesizer must be capable of generating a set of signals of certain frequencies with the stability and precision referred to a single frequency reference source. It is regarded as one of the most critical blocks in modern wireless communication systems. The following figure, Figure 2.1 shows the architecture of a typical modern transceiver, according to the source on [12]. The output signal generated by the frequency synthesizer is usually also named as the local oscillator (LO) signal, since it is used as the reference

oscillator for frequency translation and channel selection in communication systems [12].

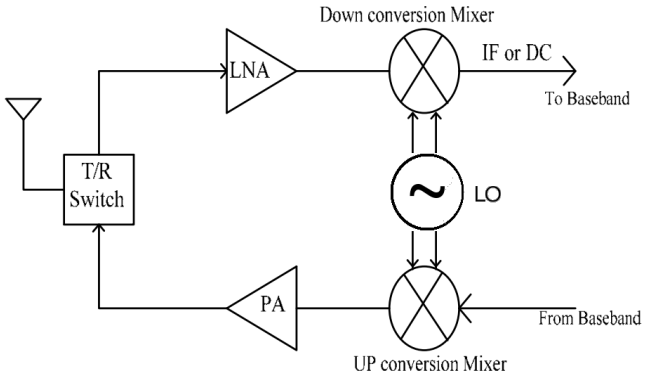


Figure 2.1: Transceiver [12]

At the receiver side, the high frequency LO signal is used to downconvert the incoming signal into a lower frequency (baseband or intermediate frequency (IF)) where it can be processed to extract the carrying information. The same LO signal can be used to upconvert the baseband signal to an RF frequency, so it can be transmitted. The LO is mainly designed to guarantee the accuracy of its output signal under the operating given conditions. The frequency synthesizer is usually implemented by using a phase-locked loop (PLL) [12].

2.2 Receiver Architectures

Receivers can be divided in three main groups:

- Conventional Heterodyne or IF receivers are the kind of receivers that use at least one IF;
- Homodyne or zero-IF receivers are the ones that convert the signal directly to the baseband;
- Low-IF receivers combine the advantages of the homodyne and conventional IF architectures [16].

2.2.1 Heterodyne or IF Receivers

The heterodyne receiver has been, for a long time the most commonly used receiver topology. With this architecture, the desired signal is downconverted from its carrier frequency to an intermediate frequency (single IF); in some cases, it is further downconverted (multi IF). The schematic of a modern IF receiver for quadrature IQ (in-phase and quadrature) signals is represented in Figure 2.2 [16].

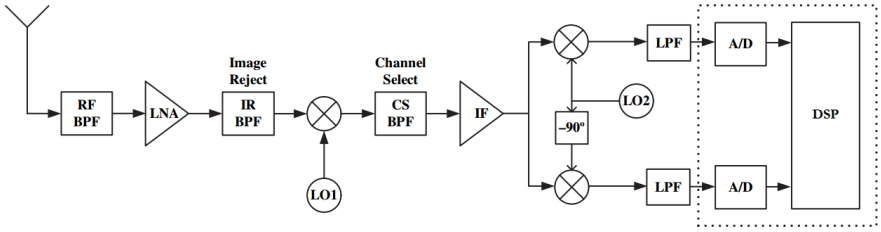


Figure 2.2: Heterodyne Receiver [16]

This receiver can be built in different technologies such as GaAs (Gallium Arsenide), bipolar, or CMOS, and uses several filters. These filters must be implemented off-chip with discrete components to achieve high Q (Quality Factor), which is very difficult or impossible to achieve with integrated components. Using these high Q elements, the heterodyne receiver achieves high performance when it comes to selectivity and sensitivity, when compared with other receiver approaches, according to [16].

This receiver is capable of handling modern modulation schemes, which require the separation of I and Q signals (In-phase and Quadrature signals)to fully recover the information, therefore accurate quadrature outputs are necessary (for conversion to the baseband). The main drawback of this receiver is that two input frequencies can produce the same IF. For example, considering that the IF is 50MHz, it is needed to downconvert a signal at 850MHz and considering a LO with 900MHz, a signal at 950MHz will be also downconverted by the mixer to the IF. This undesired generated signal is called image. To overcome this problem in conventional heterodyne receivers an image reject band-pass filter is placed before the mixer as shown in Figure 2.3 [16].

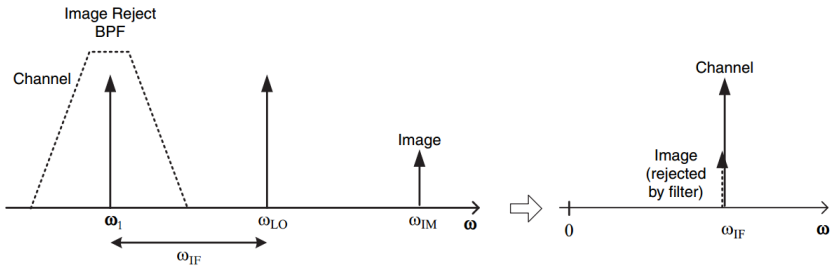


Figure 2.3: Image Rejection [16]

An important issue in heterodyne receivers to be taken account is the choice of IF. With a high IF it is easier to design the image reject filter and suppress the image. However, in addition to the image, it must be also taken in account the interferers. At the IF frequency it is required to remove interferers (which are also downconverted to the IF) using a channel select filter, as shown in Figure 2.2. Using a low IF reduces the demand on channel selection filter. Furthermore, a low IF lowers the requirements on IF amplifiers and makes the A/D converters specifications easier to fulfill; still, there is a trade-off in the heterodyne receiver: with high IF image rejection is easier, whereas with low IF the

suppression of interferers is easier.

As cited before, the heterodyne architecture described above requires the use of external components in order to have high Q. This approach is a good solution for low-cost, low area, and ultra compact modern applications. The challenge is to obtain a fully integrated receiver on a single chip. This requires either direct conversion to the baseband, or the development of new techniques to reject the image without the use of external filters [16]. These two possible approaches will be described on the next two following sections.

2.2.2 Homodyne Receivers

In homodyne receivers the RF spectrum is translated to the baseband in a single downconversion (the IF is zero). These receivers, also called "direct-conversion" or "zero-IF", are the most common approach to detect information associated with a carrier in just one conversion stage. The resulting baseband signal is then filtered with a low-pass filter, which can be integrated, to select the desired channel [16]. Since the signal and its image are separated by twice the IF, this zero IF approach implies that the desired channel is its own image, therefore the homodyne receiver does not require image rejection. All processing is performed at the baseband, and implies less requirements for filters and A/Ds. Using modern modulation schemes, the signal has information in the phase and amplitude, and the downconversion requires accurate quadrature signals. The block diagram of a homodyne receiver is shown in Figure 2.4.

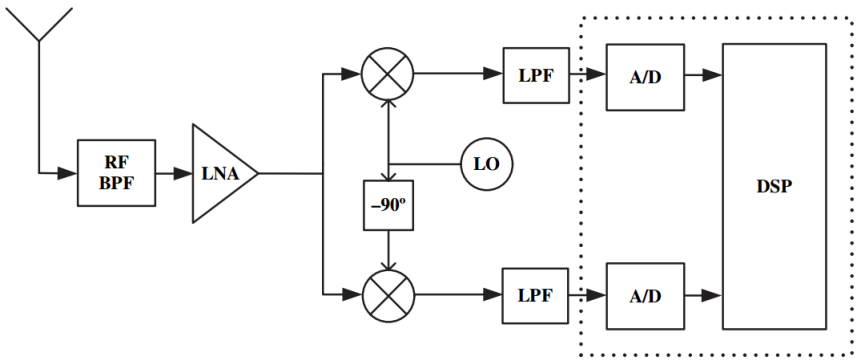


Figure 2.4: Homodyne Receiver [16]

The filter before the LNA is optional according to the reference in [16], but it is often used to suppress the noise and interference outside the receiver band. This simple approach permits a highly integrated, low area, low power, and low-cost realization. Direct conversion receivers have several disadvantages with respect to heterodyne receivers, which do not allow the use of this architecture in more demanding applications. These disadvantages are related to flicker noise, channel selection, LO (local oscillator) leakage, quadrature errors, DC offsets, and intermodulation:

- Ficker noise: The flicker noise from any active device has a spectrum close to DC. This noise can corrupt substantially the low frequency baseband signals, which is a severe problem in MOS implementation ($1/f$ corner is about 200kHz).
- Channel selection: The desired signal at the baseband must be filtered, amplified, and converted to digital domain. The low-pass filter must suppress the out-of-channel interferers; this filter is hard to implement due to its specifications taking account to low-noise and high linearity.
- LO leakage: LO signal coupled to the antenna will be radiated, and it will interfere with other receivers using the same wireless standard. To decrease this effect, it is important to use differential LO and mixer outputs to cancel common mode components.
- Quadrature error: Quadrature error and mismatches between the amplitudes of the I and Q signals corrupt the downconverted signal constellation (e.g., in QAM). This is the most critical aspect of direct-conversion receivers due to I and Q signals have different information, and it is difficult to employ accurate high frequency blocks with great quadrature relationship accuracy.
- DC offsets: Since the downconverted band extends down to zero frequency, any offset voltage can corrupt the signal and cause saturation in the receiver's baseband output stages. Therefore, DC offset removal or cancellation is required in direct-conversion receivers.
- Intermodulation: Even order distortion produces a DC offset, which is signal dependent. Thus, these receivers must have a very high IIP2 (input second harmonic intercept point).

The direct conversion approach requires very linear LNAs and mixers, high frequency local oscillators with precise quadrature outputs, and use of a method for achieving sub-microvolt offset and $1/f$ noise. All these requirements are hard to fulfill simultaneously.

2.2.3 Low-IF Receivers

Heterodyne receivers have important limitations due to the use of external image reject filters; Homodyne receivers have some drawbacks because the signal is translated directly to the baseband; Therefore, there is interest in the development of new techniques to reject the image without using filters. An architecture that combines the advantages of both the IF and the zero-IF receivers is the low-IF architecture. The low-IF receiver is an architecture based in a heterodyne receiver that uses special mixing circuits that cancel the image frequency. A high quality image reject filter is not necessary anymore and the disadvantages of the zero-IF receiver are avoided. Since image reject filters are not required, it is possible to use a low IF, allowing the integration of the whole system

on-chip. The low IF lowers the requirements in the IF channel select filter specifications, and, since it works at a relatively low frequency, it can be integrated on-chip. In a low-IF receiver the value of IF ranges from once to twice the bandwidth of the wanted signal. For example, an IF frequency of few hundred kHz can be used in GSM applications (200 kHz channel bandwidth), as described in the reference in [16]. Quadrature carriers are necessary in modern modulation schemes, and in low IF receivers they have an additional use: accurate quadrature signals are a demand to remove the image signal. This removal depends strongly on component matching and on the accuracy of LO (local oscillator) quadrature. Two image reject mixing techniques can be used, which have been proposed by Hartley and by Weaver.

2.2.3.1 Hartley Architecture

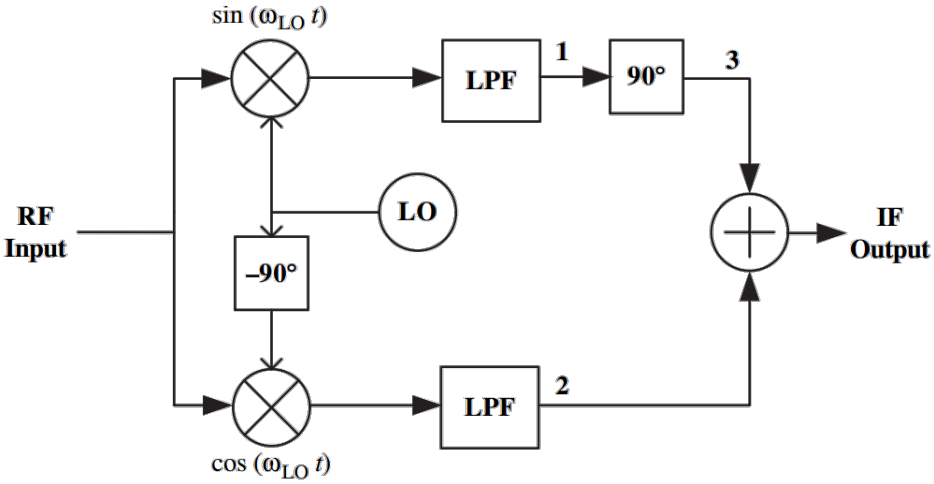


Figure 2.5: Hartley Architecture with single output[16]

The Hartley architecture has the block diagram presented in Figure 2.5. The RF signal is mixed with the quadrature outputs of the local oscillator. After low-pass filtering of both mixers' outputs, one of the resulting signals is shifted by 90°, and a subtraction is performed, as shown in Figure 2.5. In order to show the image cancellation process the points 1, 2, and 3 must be considered. It is assumed that

$$x_{RF}(t) = V_{RF}cos(\omega_{RF}t) + V_{IM}cos(\omega_{IM}t) \tag{2.1}$$

where V_{IM} and V_{RF} are, respectively, the amplitude of image and RF signals, and ω_{IM} is the image frequency. It follows that

$$x_1(t) = \frac{V_{RF}}{2}sin[(\omega_{LO} - \omega_{RF})t] + \frac{V_{IM}}{2}sin[(\omega_{LO} - \omega_{IM})t] \tag{2.2}$$

$$x_2(t) = \frac{V_{RF}}{2}cos[(\omega_{LO} - \omega_{RF})t] + \frac{V_{IM}}{2}cos[(\omega_{LO} - \omega_{IM})t] \tag{2.3}$$

Equation 2.2 can be written as:

$$x_1(t) = -\frac{V_{RF}}{2} sin[(\omega_{RF} - \omega_{LO})t] + \frac{V_{IM}}{2} sin[(\omega_{LO} - \omega_{IM})t] \tag{2.4}$$

Since a shift of 90° is equivalent to a change from $cos(t)$ to $sin(t)$:

$$x_3(t) = \frac{V_{RF}}{2} cos[(\omega_{RF} - \omega_{LO})t] - \frac{V_{IM}}{2} cos[(\omega_{LO} - \omega_{IM})t] \tag{2.5}$$

By adding the equations 2.3 and 2.5 it is possible to cancel the image band and yield the desired signal. In Hartley's approach, the quadrature downconversion followed by a 90° phase shift produces in the two paths the same polarities for the desired signal, and opposite polarities for image. The major drawback of this architecture is that the receiver is sensitive to the local oscillator quadrature errors and to mismatches in both signal paths causing incomplete image cancellation. The relationship between the image average power (P_{IM}) and the signal average power (P_S) is, according to the source on [16]:

$$\frac{P_{IM}}{P_S} = \frac{V_{IM}^2}{V_{RF}^2} \frac{(V_{LO} + \Delta V_{LO})^2 - 2V_{LO}(V_{LO} + \Delta V_{LO})cos(\theta) + V_{LO}^2}{(V_{LO} + \Delta V_{LO})^2 + 2V_{LO}(V_{LO} + \Delta V_{LO})cos(\theta) + V_{LO}^2} \tag{2.6}$$

where V_{LO} is the amplitude of the LO, ΔV_{LO} is the amplitude mismatch, and θ is the quadrature error. Noting that V_{IM}^2/V_{RF}^2 is the image-to-signal ratio at the receiver input (RF), the image rejection ratio (IRR) is defined as P_{IM}/P_S at the IF output divided by V_{IM}^2/V_{RF}^2.

$$IRR = \frac{\left.\frac{P_{IM}}{P_S}\right|_{out}}{\left.\frac{V_{IM}^2}{V_{RF}^2}\right|_{in}} \tag{2.7}$$

The resulting equation can be simplified if the mismatch is small ($\Delta V_{LO} \ll V_{LO}$) and the quadrature error θ is small, citing the font on [16]:

$$IRR \approx \frac{\left(\frac{\Delta V_{LO}}{V_{LO}}\right)^2 + \theta^2}{4} \tag{2.8}$$

Noting that have considered only errors of the amplitude and phase in the local oscillator.

Mismatches in mixers, filters, adders, and phase shifter will also contribute to the IRR. In integrated circuits, without using calibration techniques, the typical values for amplitude mismatch are 0.2-0.6 dB and for the quadrature error 3-5°, leading to an image suppression of 25 to 35 dB according to the references on [16].

2.2.3.2 Weaver Architecture

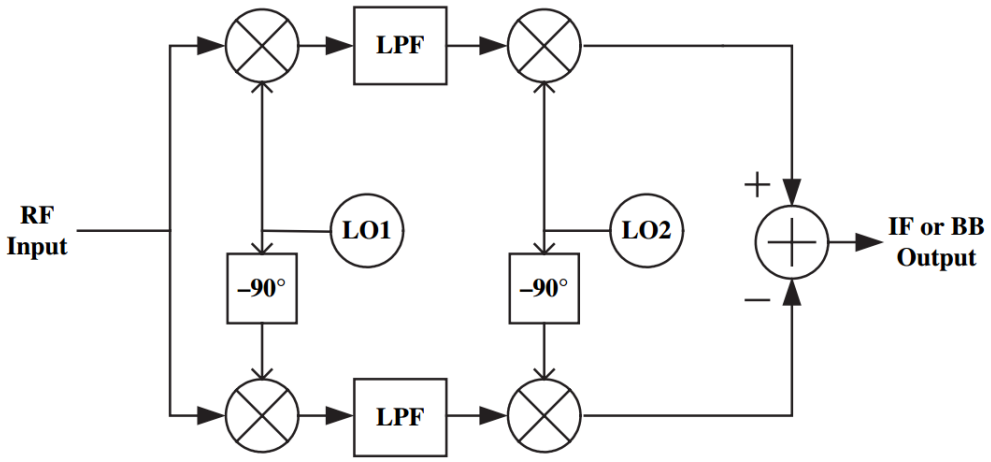


Figure 2.6: Weaver Architecture with single output [16]

The second type of image-reject mixing is performed by the Weaver architecture, presented in Figure 2.6. This is similar to the Harley architecture, but the 90° phase shift in one of the signal paths is replaced by a second mixing operation in both signal paths: the second stage of I and Q mixing has the same effect of the 90° phase shift used in the Hartley approach. As with the Hartley receiver, if the phase difference of the two local oscillator signals is not exactly 90°, the image is no longer completely canceled. The Weaver architecture has the advantage that the RC-CR mixer mismatch effect on the 90° phase shift after the downconversion in the Hartley architecture is avoided and the second order distortion in the signal path can be removed by the filters following the first mixing. However, like the Hartley architecture, the Weaver architecture is sensitive to mismatches in amplitude and quadrature error of the two LO signals. It suffers from an image problem (in the second mixing operation) if the second downconversion is not to the baseband, as shown in Figure 2.7.

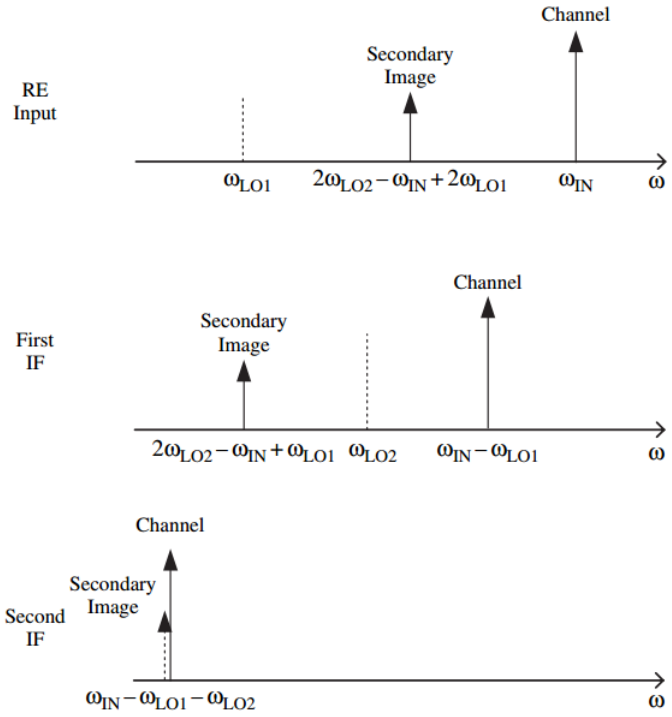


Figure 2.7: Secondary image problem in the Weaver Architecture [16]

In this case the low pass filters, must be replaced by bandpass filters, to suppress the secondary image, but, the image suppression is easier at IF than at RF.

The receiver of Figure 2.6 needs to be modified to provide baseband quadrature outputs, which are necessary in modern wireless applications. 6 mixers are required to cancel the image and separate the quadrature signals, as shown in Figure 2.8. The second two mixers in Figure 2.6 are replaced by two pairs of quadrature mixers, and their outputs are then combined. This modified Weaver architecture is usually used in low-IF receivers according to the font on [16].

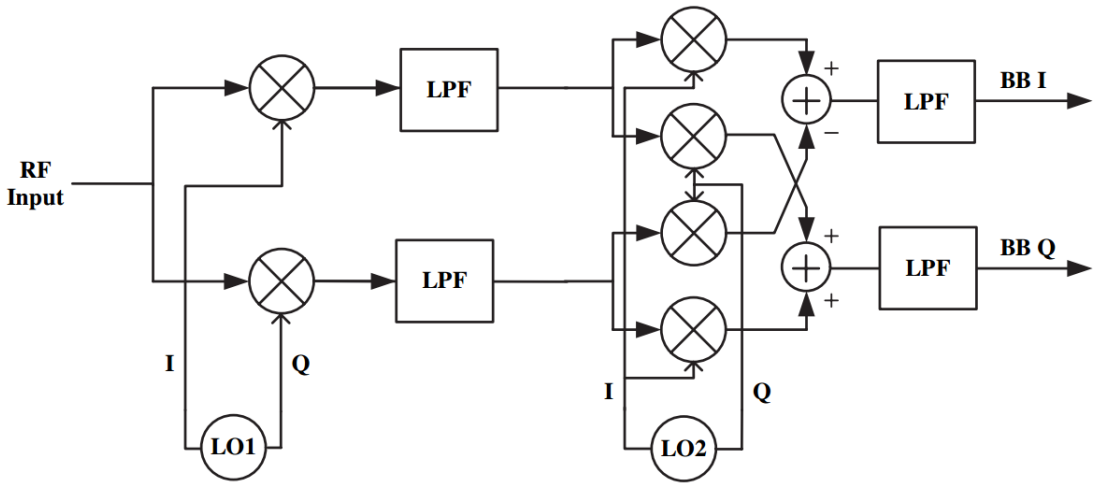


Figure 2.8: Weaver Architecture with quadrature outputs [16]

2.3 Transmitter Architecures

Transmitter architectures are usually divided in two groups:

- Heterodyne are the type of transmitters that use intermediate frequency;
- Direct upconversion are the ones that convert directly the signal to the RF band.

2.3.1 Heterodyne Transmitters

The heterodyne upconversion, presented in Figure 2.9, is the most often used architecture in transmitters. In these transmitters the baseband signals are modulated in quadrature (modern transmitters must handle quadrature signals) to the IF, once that it's easier to provide accurate quadrature outputs at IF than at RF. The IF filter that follows rejects the harmonics of the IF signal and reduces the transmitted noise [16].

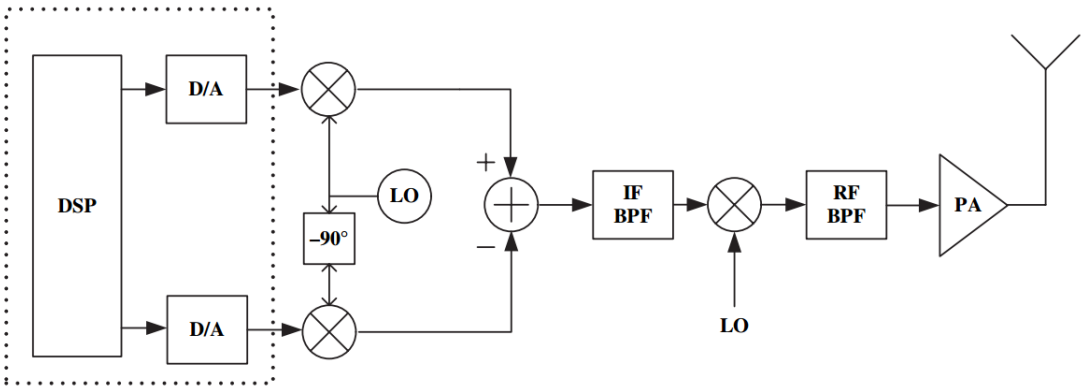


Figure 2.9: Heterodyne Transmitter [16]

The IF modulated signal is upconverted, amplified (by the power amplifier), and transmitted by the antenna. A heterodyne transmitter requires an RF band-pass filter to suppress the unwanted sideband after the upconversion regarding the spurious emission levels imposed by the standards. This filter is usually implemented passive and built with off-chip components. This topology does not allow full integration due to the off-chip passive components in IF and RF filters [16].

2.3.2 Direct Upconversion Transmitters

In this type of transmitter, shown in Figure 2.10, the baseband signal is directly upconverted to RF. The RF carrier frequency is equal to the LO frequency at the mixers input. A quadrature upconversion is required by modern modulations schemes. This topology can be fully integrated because there is no need to suppress any mirror signal generated during the upconversion, therefore there is no need for filters. As in the receiver, the local oscillator frequency is the carrier frequency, according to the source on [16].

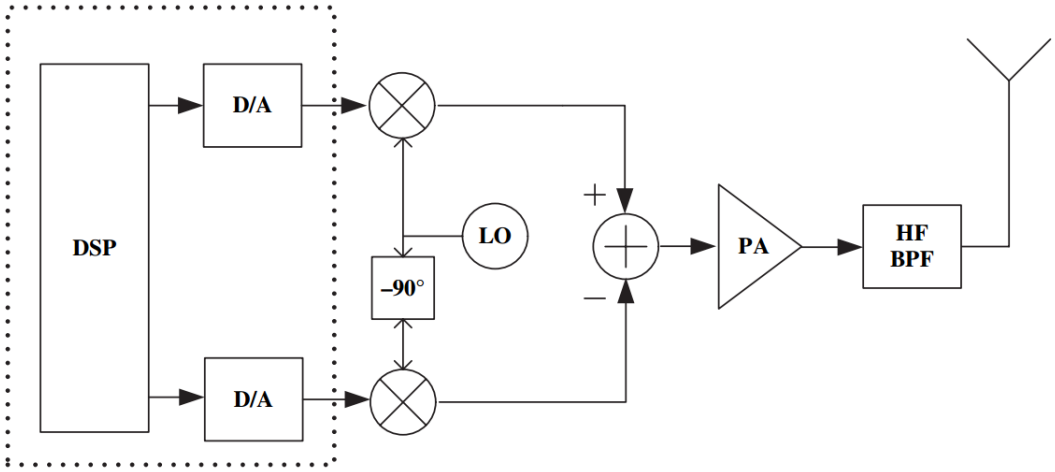


Figure 2.10: Direct Up-Conversion Transmitter [16]

The main disadvantage is the "injection pulling" or "injection locking" of the local oscillator by the high level PA output. These effects occur when an oscillator is perturbed by a second oscillator that operates in a nearby frequency. The resulting spectrum cannot be suppressed by a bandpass filter, because it has the same frequency as the wanted signal [16].

In the next chapters, an important aspect of the PLL to be considered is the Phase Noise. Its concept will be introduced and discussed. The PLL concept and its different types will also be abridged in the next chapters, along with the main blocks of the phase-locked loop (PLL), such as Voltage-Controlled Oscillator (VCO), Phase Frequency Detector (PFD), Charge Pump (CP), Frequency Divider and Loop Filter (LF).

Chapter 3

Phase-Locked Loop

A Phase-Locked Loop is a feedback system that combines a Voltage Controlled Oscillator (VCO) and a phase comparator. This combination allows the oscillator to maintain a constant phase angle relative to a reference signal.

The operation of a PLL consists in calculating the phase difference between two signals (θ_{in} and θ_{out}) and, due to the negative feedback, the phase of the output signal, θ_{out}, is adjusted so that it can synchronize with the phase of the input signal, θ_{in} [15]. Therefore, in sum, it can be concluded that the PLL must fulfill the following equations:

$$\theta_{out} = \theta_{in} \tag{3.1}$$

$$f_{ref} = N f_{out} \tag{3.2}$$

where θ_{out} and θ_{in} are the reference and output phase, f_{ref} and f_{out} are the reference and output frequencies and N is an integer value of the frequency divider.

The following figure 3.1 shows the general building blocks of a PLL:

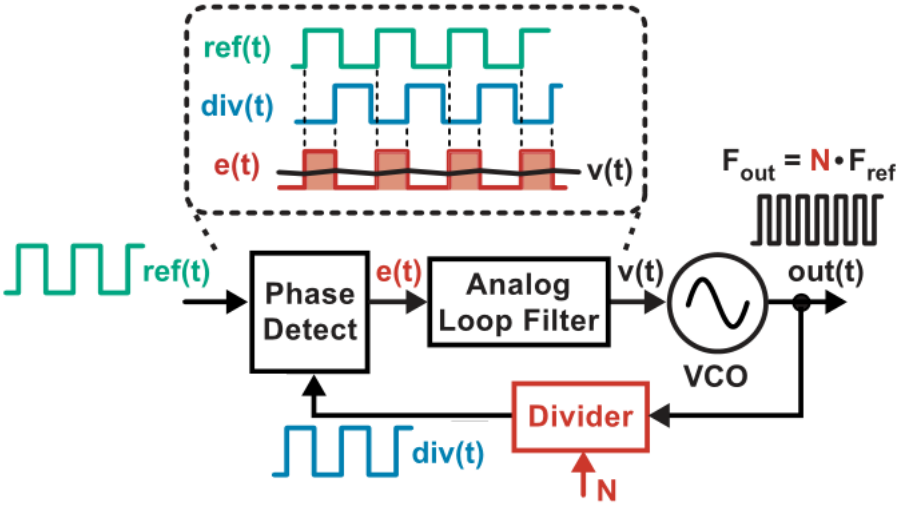


Figure 3.1: PLL block diagram [19]

- Phase Detector (PD): This is a non-linear device, used in PLLs, that produces a voltage $e(t)$ that is proportional to the phase difference between the two signals.
- Loop Filter (LF): Introducing a low pass filter in the loop allows the possibility to control the PLL bandwidth independently from the PLL static behavior.
- Voltage Controlled Oscillator (VCO): Non-linear device that can be tuned over a certain frequency range by varying its supply voltage [2].
- Divider: Allows the PLL to function as a frequency synthesizer (frequency modulation).
- Negative feedback loop: This loop allows the output signal to be connected back to the PD (divided signal, $div(t)$). The PD compares this signal with the input signal (reference signal, $ref(t)$) [2].

3.1 Classification of PLL Types

PLLs can be described in many forms, such as in Type of PLL, PLL order or even PLL technology.

The PLL were implemented in the second quarter of the 20th century and only when they became available as IC there were found broader applications to them. The first IC PLLs were entirely made of analog devices: an analog multiplier was used as phase detector, the loop filter was build on passive or active RC filter and the VCO was used to generate the output signal of the PLL. This type of PLL is usually refered as Analog PLL (APLL) or Linear PLL (LPLL) [3]. These are Type-I PLLs.

Taking a quick leap into the future, the PLL entered the digital domain, making therefore the Digital PLL (DPLL). It is usually named as an "hybrid"PLL due to only the

phase detector being built by a digital circuit. These digital phase detectors are usually EXOR gates, JK or D Flipflops. When the phase detector is based in D Flipflops, it is considered that the PLL is a Type-II PLL due to its characteristics, as shown in 5.3.3.

Some years later, the All-Digital PLL (ADPLL) was invented. This PLL is exclusively built with digital blocks, therefore does not contain any passive components such as resistors or capacitors [3].

Though there are other kind of PLLs such as the Software PLL (SPLL), it is possible to say that these are not built from actual specialized hardware, but are programmable and can simulate any kind of PLL.

The next subsection will only abridge the PLLs based on electronic devices with great emphasis on the DPLL, which was the architecture developed for this thesis.

3.1.1 Analog or Linear PLL

Different PLL types are built from different blocks. To design a LPLL it is necessary to implement the appropriate circuits implementing the functions on the Figure 3.1.

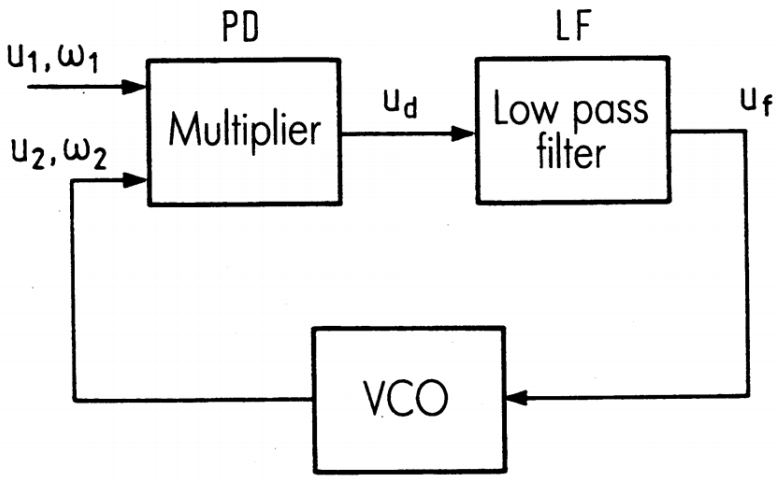


Figure 3.2: LPLL block diagram [3]

In LPLLs, a four-quadrant multiplier (can have simultaneously positive or negative inputs or outputs) or a mixer is used as a phase detector to detect the input signal, represented in the previous Figure 3.2 as U_i (with a certain frequency ω_i) and compare it to U_o (also with a frequency ω_o). The difference between those two signals generates a voltage depending on the phase error. In a locked state, both frequencies are equal. A loop filter, used fo filter high frequency signals and noise from the phase detector helps stabilizing the system and transforms the phase difference into a voltage to adjust the oscillation frequency coming from the VCO. These loop filters are low pass filters usually composed by active or passive components. The Voltage Controlled Oscillator is an analog oscillator

controlled by a certain voltage which generates a relative oscillation frequency in a fixed range.

The input of the phase detector includes the input signal of the PLL and the output signal of the VCO, as shown in the Figure 3.2. Once the phase detector of the LPLL is a four-quadrant analog multiplier or mixer, only the phase difference is detected. The output signal of the phase detector is a product of the signals u_i and u_o. The product results in a signal which contain an higher frequency component and a lower frequency component, $u_d(\theta_1 + \theta_2)$ and $U_d(\theta_1 - \theta_2)$, respectively. This signal is filtered by the loop filter in order to remove the higher frequency component and use the lower one to control the VCO frequency. In order for the PLL to be locked θ_1 must be equal to θ_2).

The LPLL is the initial figure demonstrated above. However, due to the low output frequency range, long locking time and large phase error in comparison to other digital or hybrid approaches, it is not usually used in modern designs.

3.1.2 Digital PLL

As mentioned before, the DPLL is a hybrid system built from both analog and digital blocks. The only block that is fully digital is the phase detector. In many ways the DPLL works similarly to the analog PLL therefore the some of the same theoretical approach can be applied, but in other aspects the DPLL has a completelly different behavior. It is considered that the DPLL is more similar to the analog PLL than the ADPLL.

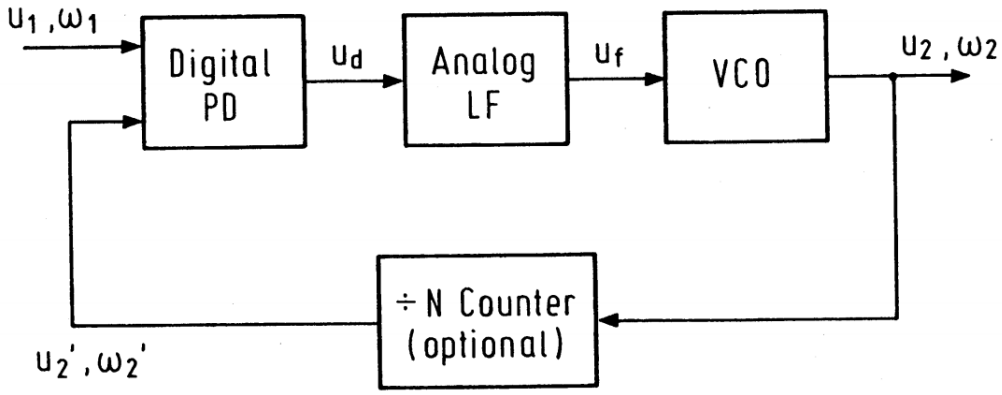


Figure 3.3: DPLL block diagram [3]

The block diagram of the DPLL is show in the previous Figure 3.3. Similarly to the LPLL, it consists of the three previously mentioned blocks, the phase detector, loop filter and voltage-controlled oscillator. In many DPLL applications (e.g., PLL frequency synthesizers) a divide-by-N counter is inserted between the VCO and the phase detector. It is usually also named as N-divider. When such component is used, at its output, the signal u_2' is N times the VCO frequency (making then $\omega_2 = N\omega_2'$). The loop filter and VCO remain the same type of blocks previously mentioned. In this special kind of PLL, a number of different logical circuits can be used as a phase detector. The three more

used and more important are represented in the Figure 5.10 on Chapter 5. The remaining work principle is similar to LPLL.

3.1.3 All-Digital PLL

As implied by the name, the all-digital phase-locked loop operates in an all-digital signal environment [3]. The analog signal of the VCO must be replaced by its digital counterpart: the digital signal of an digital controlled oscillator (DCO). Also, by replacing the analog filter with a the digital filter, the whole system becomes an all-digital phase-locked loop. Due to the absence of passive devices, this kind of PLL has low noise interference and increased stability [3].

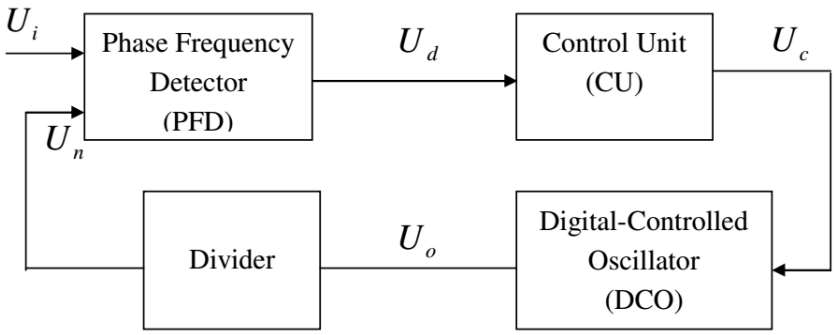


Figure 3.4: All-Digital PLL [7]

The Figure 3.4 presents the basic structure of an all-digital PLL. The phase-frequency detector consists of various digital logic circuits which produce discrepancy of two input signal phase, like the previous PFD in 5.18a. After receiving the generated results of the PFD, the control unit processes the signal and then controls DCO to generate the required frequency.

3.2 PLL Comparison

All of the mentioned PLLS have many advantages and disadvantages. They are compared and illustrated in Table 3.1.

These advantages and disadvantages are mainly separated by the design methodology. The PLL designed with analog components has truthly the characteristics of analog circuits. In opposition, the ADPLL designed with digital circuits has characteristics of digital circuits. The digital circuits have higher noise immunity than the analog circuits. The VCO of an analog PLL or a DPLL produces a continuous frequency band while the DCO of an ADPLL produces a discrete frequency band. The VCO has higher resolution than the DCO. The digital circuits generally have lower power consumption than the analog circuits. An ADPLL may have small area because the loop filter of an analog PLL or a DPLL usually have one or more large capacitors that occupy large area that cannot be

Table 3.1: PLL Comparison

	Analog PLL	Digital PLL	All-Digital PLL
Design Methodology	Analog	Analog and Digital	Digital
Noise Immunity	Low	Low	High
Oscillation Frequency	High	High	Low
Oscillator Range	High	High	Low
Lock Time	Long	Long	Short
Power Consumption	Large	Large	Small
Occupied Area	Large	Large	Small

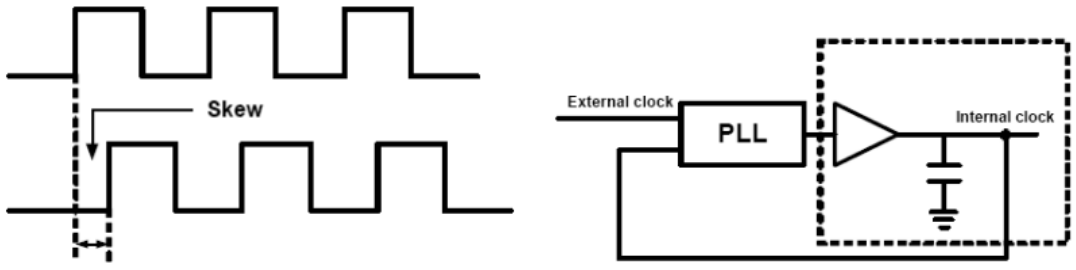
reduced as the process technology improves. An ADPLL shortens its lock time by dealing with digital signals.

3.3 PLL uses

PLLs are widely used in RF applications, television and noise cancelers. Besides the previously referred use as an LO, they can also be used in carrier recovery, clock skew suppression, tracking filters, frequency and phase demodulation, phase modulation, frequency synthesis, and clock synchronization [2].

3.3.1 Clock Skew Suppression

Figure is the representation of clock skew. Clock skew usually happens in the high speed systems owing to the delay of wire in the chips or interconnected capacitance. It can be reduced by using a PLL as shown in [7].



a Clock Skew b Clock Skew Suppression Technique

Figure 3.5: Clock Skew Suppression [7]

3.3.2 Jitter Reduction

Jitter a statistical the deviation from precise clock transition as shown in Figure 3.6. The dotted line represents the correct clock transition and the solid line means that the clock

suffered from with a deviation of Δt. In general, the jitter phenomenon can be reduced efficiently by the PLL.

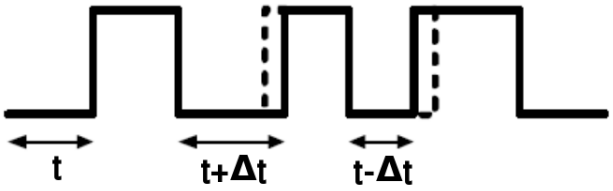


Figure 3.6: Jitter [7]

3.3.3 Frequency Synthesizer

Many applications require frequency multiplication. A high frequency and high Q factor in modern applications is not easy to achieve unless area and power consumption are despised, but a PLL with frequency synthesizing function can achieve frequency multiplication efficiently.

3.3.4 Clock and Data Recovery

In a data transmission system, the data may be interfered by noise or the clock information may not be transferred, so it needs to be extracted from the data. The PLL is useful to achieve this purpose. Figure 3.7 illustrates an example, the noisy data enters clock recovery circuit and cooperates with a D Flipflop to extract the precise data.

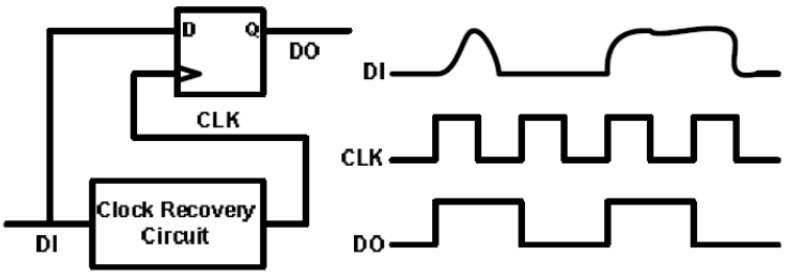


Figure 3.7: An example of Clock and Data recovery circuit [7]

Chapters 4 will introduce the concept of oscillators and many of their uses, such as quadrature and differential uses in order to compare them both. Sections 5.1 and 5.2 will introduce and study the blocks shown in Figure 3.1, except for the phase detector, already abridged in 5.3.3.

CHAPTER 4

OSCILLATOR

An oscillator is an electronic circuit that generates an oscillating periodic signal, usually a sin wave or a square wave. The oscillator transforms a DC signal from a power supply into an alternate current signal (AC).

They are widely used in several electronic devices such as radios, transmitters, periodic signal generators (clocks) and are usually defined by its output signal frequency [5].

The basic structure of an oscillator consists in two blocks: an amplification block, A, with positive feedback and a frequency-selective network, β, as it is shown on the following picture:

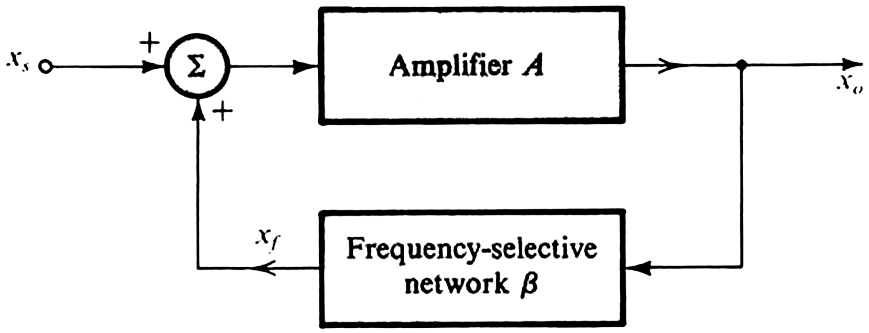


Figure 4.1: Oscillator Block [18]

On a real oscillator, the X_s input value does not exist, because the circuit goes into an auto-oscillation estate. X_s is an introduction variable that helps to understand the operation principle of the oscillator. In our case, we will have two possible initial states, 0 and 1. X_s will have one of those values in $t = 0$.

Oscillations occur even without an input value. They are initiated when the amplification block is powered up. Due to electronic noise coming from that block (whose value

is low, near zero; but not zero), the oscillations are initiated. The noise is amplified by the inverters and filtered by the B block until it converges into a sinusoidal or square wave, at a certain frequency.

The β block previously shown on the figure consists in a frequency-selective network (or filter). Many examples can be named, such as RC circuits. Joining the amplifier block, it can be made a phase-shift oscillator or a Wein Bridge Oscillator. In our case, the β block does not exist. The output of the inverter chain is connected directly to the input of itself.

According to the previous figure, the gain A with the positive feedback can be defined as function of the β block and the A block, therefore:

$$L(s) = \frac{A(s)}{1 - A(s)\beta(s)}. \tag{4.1}$$

4.1 Barkhausen Criterion for Oscillation

Once that the equation is the denominator of the open loop gain expression, $L(s)$, we can conclude that for a certain frequency, f_{osc}, it is possible that the open loop gain stays $A\beta$=1, and the closed loop gain will be infinite.

Therefore, for the frequency f_{osc} the circuit has a finite output even for a null input, this is, the circuit will enter an auto-oscillation state.

Any circuit that presents these characteristics is, by definition, an oscillator.

The condition for a circuit from the previous figure to supply a sinusoidal wave at the output, on the frequency f_{osc}, it is necessary that:

$$L(jw_0) = A(jw_0)\beta(jw_0) = 1. \tag{4.2}$$

This is, at w_0, the phase of the open loop gain must be zero and the amplitude of the gain in open loop must be unitary:

$$A\beta = 1 \tag{4.3}$$

and

$$\angle A\beta = 2k\pi. \tag{4.4}$$

These conditions are known as "Barkhausen Criterion". Note that for a circuit to oscillate at a certain frequency, the Barkhausen criteria must be only satisfied at a frequency w_0, else the output of the oscillator will not be a sinusoidal wave.

In fact, for a circuit to produce stable oscillations at a frequency w_0, it is necessary that the characteristic equation has its roots on $s = \pm jw_0$, demanding that $1 - A\beta(s)$ has a factor of the type $s^2 + w_0^2$.

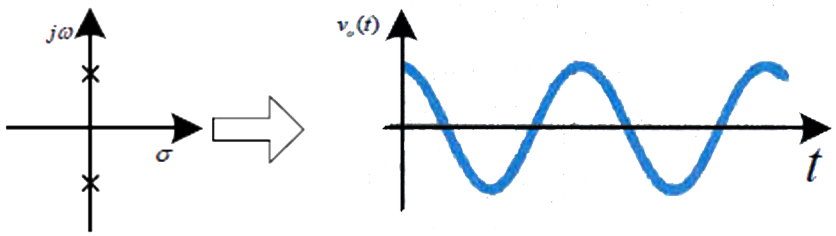


Figure 4.2: Stable Condition for Oscillations [18]

It is stated that the Barkhausen criterion is a necessary but insufficient criterion for ready state oscillation of an electronic circuit.

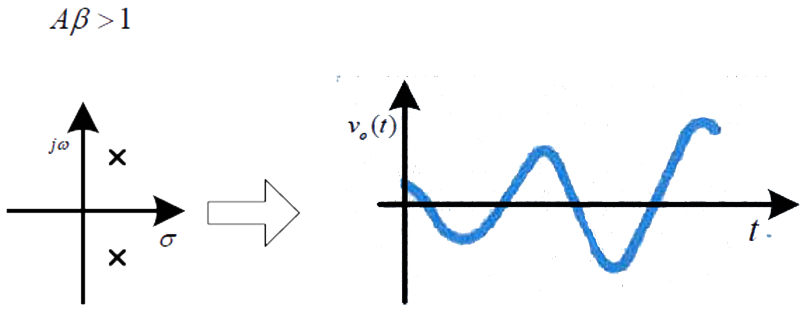


Figure 4.3: Condition to Start Oscillations [18]

On an initial state, the $L(s)$ poles must be on the right side of the complex plane, so the oscillations may start. After that, the circuit must be stabilized and be forced so $A\beta$ must be equal to 1 and the Barkhausen criteria be fulfilled to maintain the amplitude of the oscillations (instead of growing to the infinity). This is dealt to a non-linear circuit to control the amplifier gain. This circuit limits the amplitude of the oscillations and makes the open-loop gain unitary; the $L(s)$ poles are dislocated to the imaginary axis (jw) [16].

For any reason, if the $A\beta$ gain starts to decrease, this action will be detected by the non-linear circuit and it will make $A\beta$ increase to 1 again.

4.2 Types Of Oscillators

In this thesis, only the most common oscillators are introduced and they are based on CMOS technology. Therefore they may be classified into two categories:

- Quasi-Linear or Harmonic Oscillators
- Non-Linear or Relaxation Oscillators

4.2.1 Quasi-Linear or Harmonic Oscillators

These kind of oscillators produce a sinusoidal wave. There are some kinds of harmonic oscillators such as:

- RC Oscillators
- LC Oscillators
- Crystal Oscillators

4.2.1.1 RC Oscillators

These kind of oscillators contain resistors and capacitors and are used to produce low frequency signals or audio signals; they are also known as audio-frequency oscillators. Examples of these type of oscillators are Phase-Shift and Wein-Bridge Oscillators.

4.2.2 LC Oscillator

To illustrate the Barkhausen criterion, the LC oscillator can be used because it is a quasi-linear oscillator. As it is know, oscillation will occur at the frequency for which the amplitude of the loop gain is 1 and the phase is 0 [16].

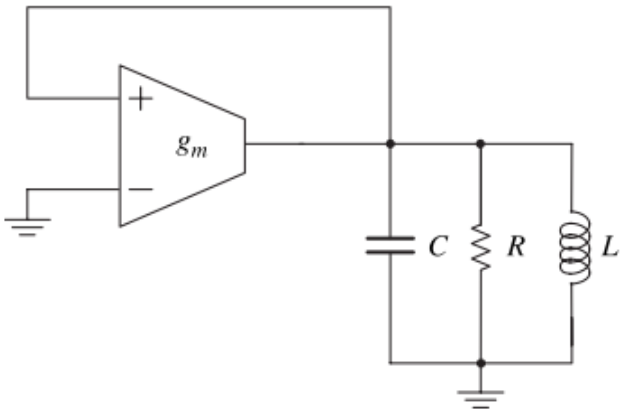


Figure 4.4: LC oscillator behavioural model [16]

A model of the LC oscillator is represented in the figure above, Figure 4.4 and its transfer function is

$$H(j\omega) = g_m \tag{4.5}$$

and $\beta(j\omega)$ is the impedance of the parallel RLC circuit:

$$\beta(j\omega) = \frac{R}{1 + j\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)Q} \tag{4.6}$$

where Q is the quality factor given by

$$Q = R\sqrt{\frac{C}{L}} \tag{4.7}$$

and ω_0 is the oscillation frequency, given by

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{4.8}$$

At the resonance frequency, the inductor and the capacitor admittances cancel and make the loop gain

$$|H(j\omega_0)\beta(j\omega_0)| = g_m R = 1. \tag{4.9}$$

The active circuit has a negative resistance, compensating the resistance of the RLC parallel. This condition is necessary but not sufficient because the loop gain must be higher than 1 for the oscillation to start, making then $g_m > \frac{1}{R}$ [16].

4.2.2.1 CMOS implementation of LC Oscillator

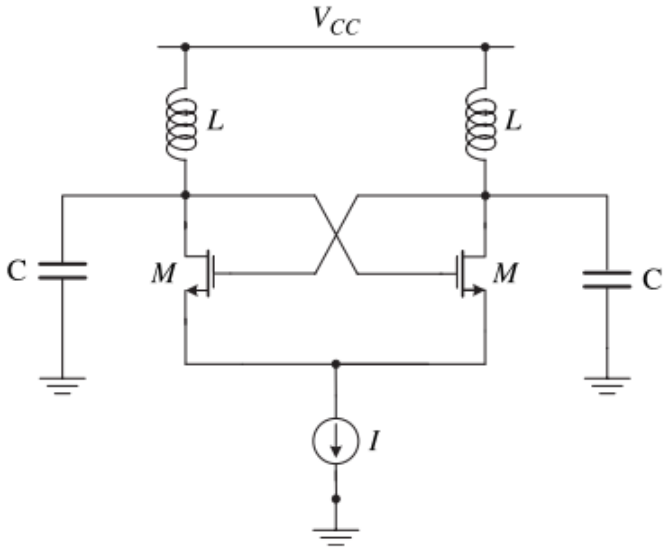


Figure 4.5: CMOS LC Oscillator with LC tank [16]

In the previous figure, Figure 4.5, a typical LC oscillator is show; it is also called differential CMOS LC oscillator, or negative gm oscillator and is widely used in RF transceivers.

The cross-coupled NMOS transistors generate a negative resistance, which is in parallel with the lossy LC tank [16].

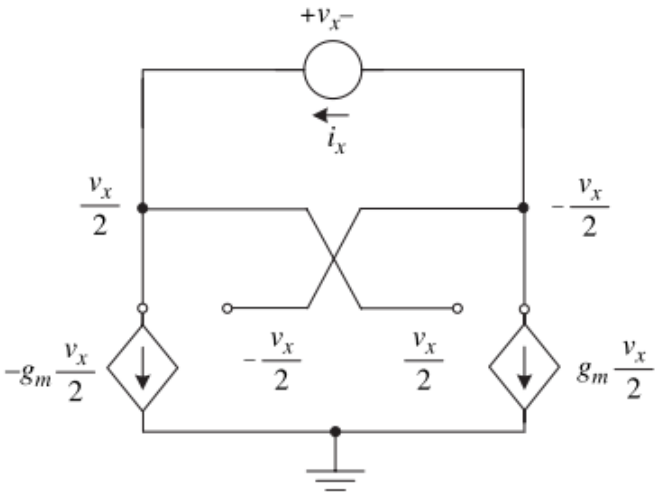


Figure 4.6: Equivalent resistance of the differential pair [16]

In the previous figure, Figure 4.6 the small signal model of the differential pair is shown. Since the circuit is symmetric, the controlled sources have the currents shown in Figure 4.6, and the equivalent resistance of the differential pair is [16]:

$$R_x = \frac{v_x}{i_x} = -\frac{2}{g_m}, \tag{4.10}$$

therefore, the differential pair realizes a negative resistance (Fig. 2.21) that compensates the losses in the tank circuit [16].

4.2.2.2 Quadrature LC Oscillator

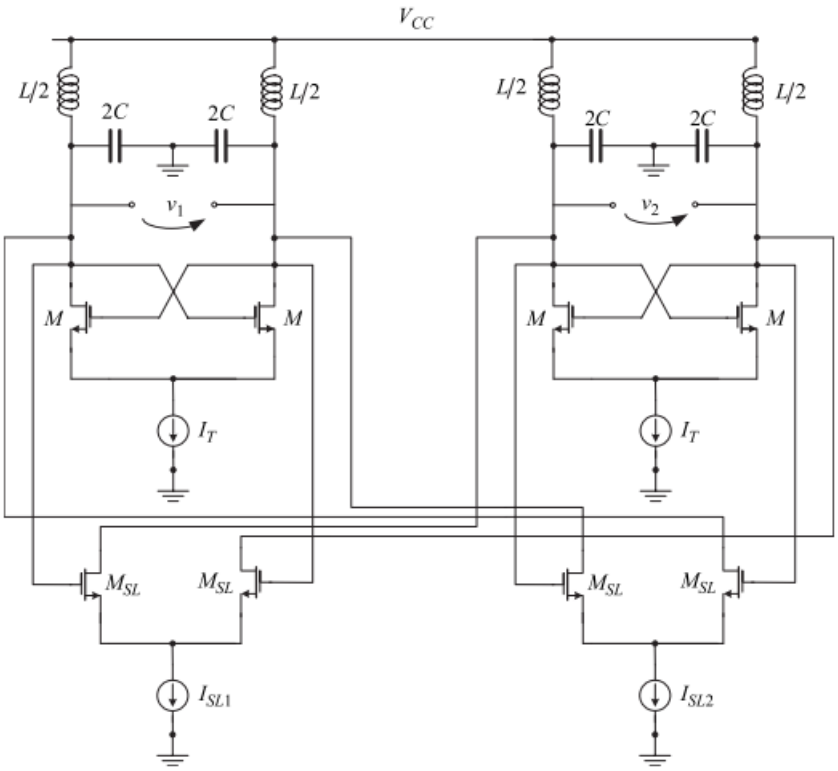


Figure 4.7: Quadrature LC Oscillator [16]

The simplest and most used implementation of the LC oscillator uses transistors to generate the negative conductance as represented in Figure 4.5. The implementation in Figure 4.7 couples two equal LC oscillators. The coupling block is implemented, as in the relaxation oscillator, with a differential pair that senses the voltage at one oscillator output and injects a current in the second oscillator, in order to trigger it. A linear model of a cross-coupled LC oscillator consists of two coupled parallel RLC circuits as represented in the next Figure, Figure 4.8. Considering that this circuit has no mismatches, all the capacitors are passive components such as capacitors, inductors and resistors are considered equal, therefore making $C_1 = C_2 = C$, $L_1 = L_2 = L$, and $R_{p1} = R_{p2} = Rp$. In parallel with each tank there are negative resistances $-1/g_m$ that cancel the losses. Two differential transconductances g_{mc} provide the coupling and the are responsible for the quadrature outputs.

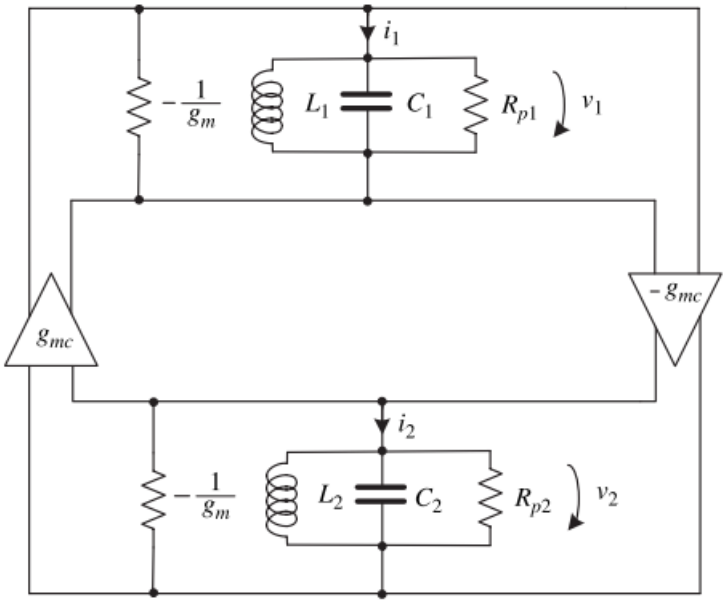


Figure 4.8: Quadrature LC Oscillator linear model [16]

In the linear model represented in the Figure 4.8,the loop gain is:

$$G_{loop}(s) = -g_{mc}^2 \left(\frac{sL}{1 + sL\left(\frac{1}{R_p} - g_m\right) + s^2 LC} \right)^2. \tag{4.11}$$

Using the Barkhausen criterion for the loop gain, equating to 1 with $g_m = 1/R_p$ and solving in order to ω ($s = j\omega$).

$$\pm j = \frac{g_{mc} sL}{1 + s^2 LC} \xrightarrow{s=j\omega} \pm 1 = \frac{g_{mc}\omega L}{1 - \omega^2 LC} \leftrightarrow \tag{4.12}$$

$$\leftrightarrow \omega^2 \pm \frac{g_{mc}}{2C} 2\omega L - \omega_0^2 = 0. \tag{4.13}$$

Making therefore possible to obtain two solutions for the oscillation frequency:

$$\omega_{osc1} = \frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}} \tag{4.14}$$

and

$$\omega_{osc2} = -\frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}}. \tag{4.15}$$

4.3 Non-Linear or Relaxation Oscillators

These oscillators are widely used in fully integrated circuits because they have no inductors and characterized by providing an output that is a non-sinusoidal wave. Instead they

produce square, rectangular or saw tooth wave forms. These kind of oscillators cannot be determined by the Barkhausen criterium and are usually used as a part of a phase-locked loop.These include the ring oscillator, explained in subsection 5.1.1.

4.3.1 RC Relaxation Oscillator

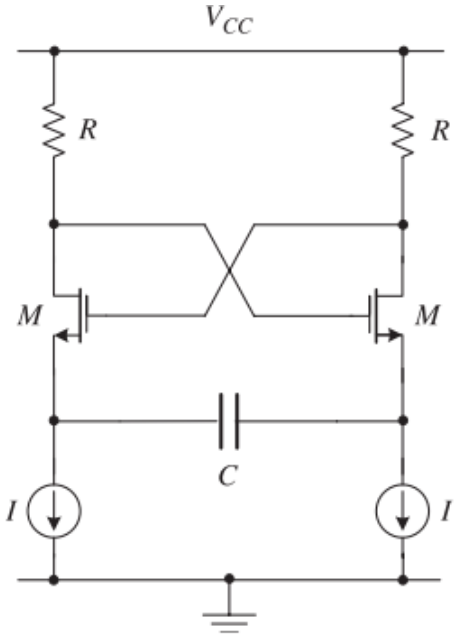


Figure 4.9: RC Relaxation oscillator [16]

Its *modus operandi* is based on the charge and discharge of the capacitor between two threshold voltage levels set internally. The oscillation frequency is inversely proportional to the circuit's capacitance [16].

Figure 4.10: Relaxation oscillator block diagram [16]

The previous image, Figure 4.10 shows the block of a relaxation oscillator, that can be modelled using an integrator and a Schmitt-trigger. The Schmitt-trigger is a memory element, and controls (switches) the sign of the integration constant.

The waveforms resultant from that oscillator are represented in the following figure, Figure 4.11. The triangular waveform is the integrator output and the square waveform is the Schmitt-Trigger output [16].

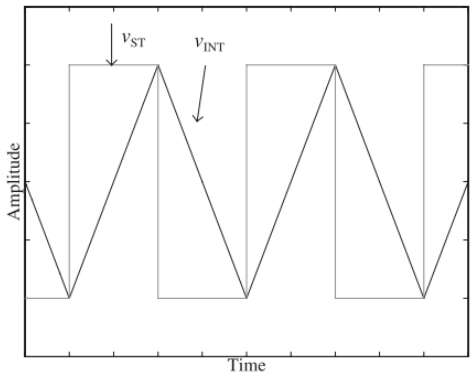


Figure 4.11: Relaxation oscillator waveforms [16]

In order to implement the oscillator at high frequencies, a simple circuit is needed. Therefore the blocks depicted in Figure 4.10 must be replaced by simple circuits that correspond to those blocks. The integrator is implemented by a capacitor, where i_c is the current that flows through that capacitor making it its input; and v_c the capacitor voltage, its output.

This voltage is the input of the Schmitt-trigger and its output is i_c. The transfer characteristic is shown on Figure 4.12. It is assumed that the switching occurs abruptly when the sign of $V_{gs1} - V_{gs2}$ changes [16].

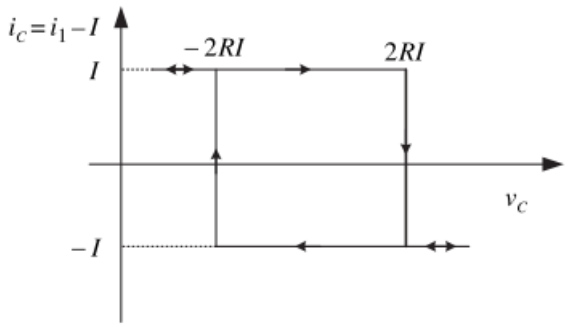


Figure 4.12: Schmitt-trigger transfer characteristic [16]

Using this approach, it can be justified the implementation of the high level diagram. There is no simplest representation, thus it can be used for RF applications.

For the oscillator output $v_{out} = v_1 - v_2$, where v_1 is the gate voltage of the transistor on the right and v_2 is the gate voltage of the transistor on the left, with $4RI$ of amplitude and i_c is the Schmitt-trigger output [16].

This oscillator integration constant is I/C (slope of v_c), and the amplitude is $4IR$. Therefore, the oscillation frequency is given by:

$$f_0 = \frac{I}{2C(4RI)} = \frac{1}{8RC}. \tag{4.16}$$

4.3.2 Two-Integrator Oscillator

The oscillator in the following figure, Figure 4.13 is composed of two-integrators and two hard-limiters that implement the sign function, connected in a feedback loop. Each integrator output determines the input polarity of the next integrator. The oscillation frequency is directly proportional to the integrators' constant and depends on the amplitude. The waveforms are rectangular at the hard-limiter outputs, and are triangular at the integrators outputs [16].

The oscillation amplitude V_{out} is the sum of the two initial values. The oscillation frequency and the amplitude are related by [16]:

$$f_0 = \frac{K_i}{2V_{out}} \tag{4.17}$$

where K_i is the integration constant and V_{out} is the output amplitude. It is known that with different integration constants, the outputs of the integrator are different, but have the same frequency and are in quadrature [16].

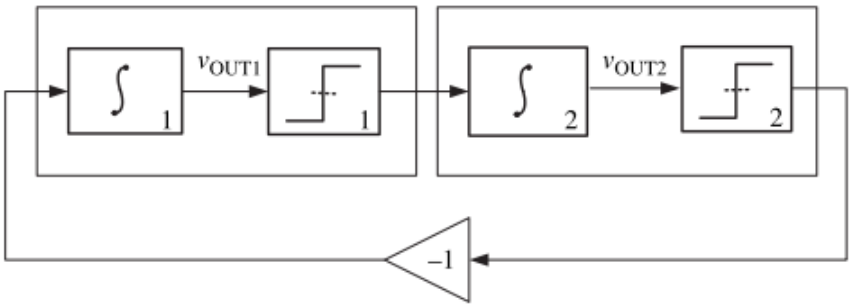


Figure 4.13: Two-integrator oscillator with hard-limiters [16]

The integrator output amplitudes are dependent on the initial conditions of two-integrators and on their integration constants [16]:

$$V_{out1} = 2\left(V_{int1} + \frac{K_{i1}}{K_{i2}} V_{int2}\right) \tag{4.18}$$

$$V_{out2} = 2\left(V_{int2} + \frac{K_{i2}}{K_{i1}} V_{int1}\right) \tag{4.19}$$

where V_{int1} and V_{int2} are the initial values. To determine the oscillation frequency, one of the previous equations () can be substituted in the equation , making the oscillation frequency [16]:

$$f_0 = \frac{1}{4\left(\frac{V_{int1}}{K_{i1}} + \frac{V_{int2}}{K_{i2}}\right)}. \tag{4.20}$$

In the high level model depicted in the figure the amplitude and frequency are defined by the initial integrator values [16].

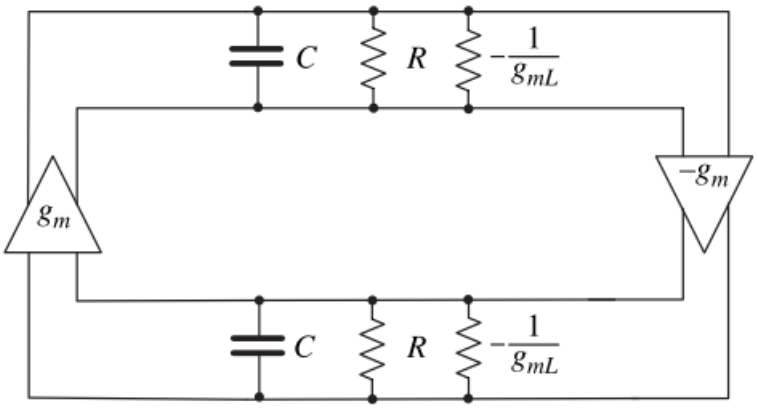


Figure 4.14: Two Integrator linear model [16]

From the model in the previous Figure, Figure 4.14, valid for quasi-linear performance, it is possible to obtain the oscillator frequency using the loop gain of the oscillator. For oscillation, the losses must be compensated ($Rp = 1/g_m L$), each stage is a perfect integrator, and the phase condition is achieved for all frequencies, because each stage of the two-integrator oscillator gives a 90 deg phase shift, as it is required for quadrature outputs. Therefore, the two-integrator oscillation frequency is determined by the amplitude condition. The loop gain is given by [16]:

$$|H(j\omega)| = \frac{g_m^2}{\omega^2 C^2} \tag{4.21}$$

and by using the amplitude condition $|H(j\omega)| = 1$, the oscillation frequency is

$$\omega_0 = \frac{g_m}{C}. \tag{4.22}$$

From the previous equation it is possible to conclude that the oscillator frequency varies by changing either the capacitance or the transconductance.

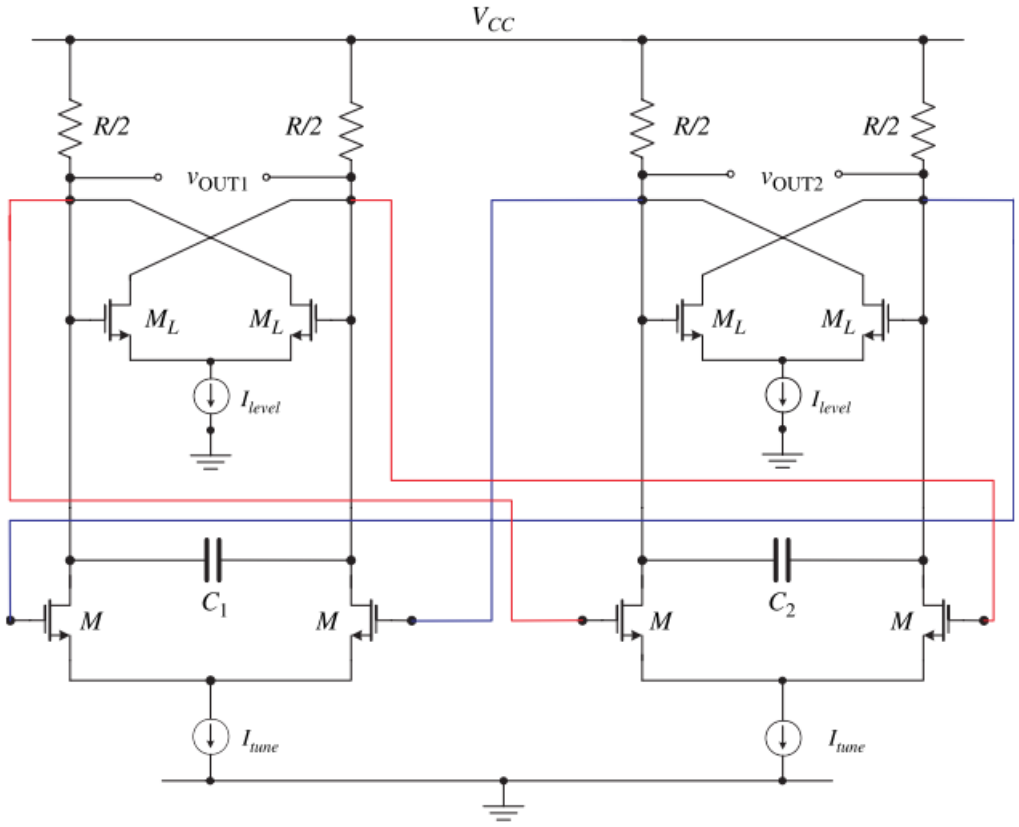


Figure 4.15: Two Integrator Circuit [16]

In a practical circuit usually varactors are used to change the capacitance or, most commonly, it is possible to change the tuning current and therefore the transconductance. With the second approach, if the transconductances are implemented with MOS transistors the frequency will be proportional to the square root of the tail current. Since it is possible to change the transconductance in a wide range, these oscillations have wide tuning range. The circuit of Figure 4.15 can work in two different modes:

- If I_{level} is increased in order to over-compensate the losses, the performance is non-linear and resembles that of the block diagram in Figure 4.10. With a strong non-linear performance (the transistors operate as switches) the waveforms are approximately triangular. In this case the oscillator amplitude is [16]:

$$V_{out} \cong I_{level} R \tag{4.23}$$

and using the equation 4.3.2 it is possible to obtain the oscillation frequency:

$$f_0 = \frac{I_{tune}}{2CV_{out}}. \tag{4.24}$$

In this case the oscillator has a behaviour similar to that of a relaxation oscillator [16].

- If the losses are compensated only to the amount necessary for the oscillations to start, the circuit of the Figure 4.15 is modelled by that of Figure 4.14. The transistors work in the linear region, and the outputs are close to sinusoidal with the amplitude that satisfies the condition $\frac{1}{g_m L} = R$.

  Once the linear operation has been assumed, the currents in the transistors of the differential pair do not reach the value of the source current I_{level}, represented in the next Figure, Figure 4.16. However, in practice the output amplitude can be approximated as

$$V_{out} \cong I_{level} R \tag{4.25}$$

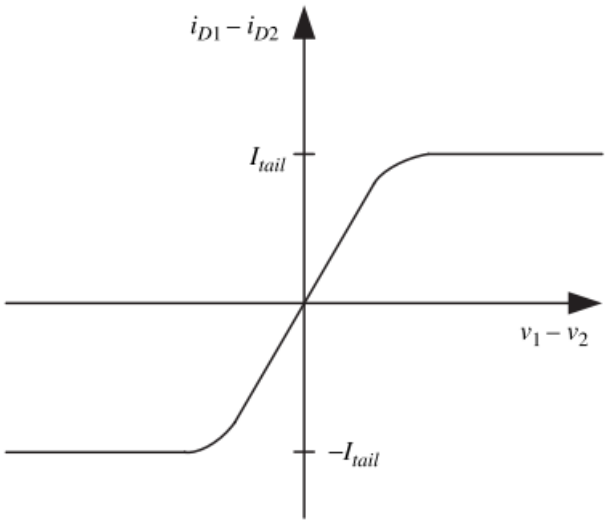


Figure 4.16: Differential voltage to current transfer characteristic of a differential pair [16]

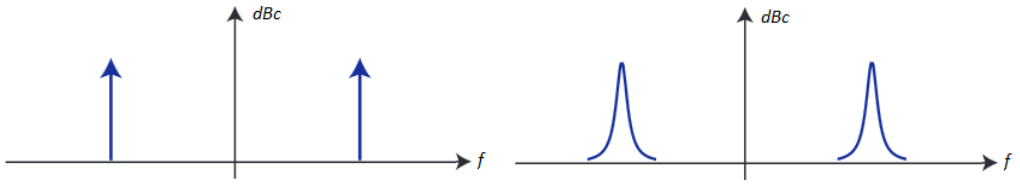
4.4 Phase Noise and Jitter

Two main aspects to be considered while designing a PLL and/or a VCO are the Phase Noise and Jitter. These two aspects are considered as random deviations of a "pure"sinusoidal wave caused by instabilities. Phase noise is a frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform caused by time domain instabilities, named Jitter.

4.4.1 Phase Noise

In transceiver applications, one of the most important aspects to be considered while projecting an oscillator is the phase-noise. The noise generated at the oscillator output causes random fluctuation of the output amplitude and phase. This noise is generated due to the oscillator non-idealism. Although it is considered that the closed-loop gain this system is infinite, since $A = 1$, in reality noise is generated on any oscillator. In sum,

phase noise is undesirable phase fluctuations due to intrinsic device noise because output power is not concentrated at the carrier frequency alone [16].



a Ideal Oscillator Spectrum b Real Oscillator Spectrum

Figure 4.17: Ideal Spectrum of an Oscillator output vs Ideal Spectrum of an Oscillator output [13]

It is said that the noise in the spectrum is due to "phase" noise rather than amplitude noise. An oscillator has a well defined amplitude which is controlled by the non-linearity of the circuit. If there is an amplitude perturbation, it is naturally rejected by the oscillator. Once again, this occurs because the oscillation occurs at a frequency when the loop gain is unity. If the amplitude grows, due to compressive characteristics of the non-linearity, the loop gain decreases and the oscillation amplitude dampens. Likewise, if the amplitude drops, the loop gain goes over unity due to expansive characteristics of the non-linearity, and the amplitude grows back. The phase of the oscillator, on the other hand, is "free running". Any phase-shifted solution to the oscillator is a valid solution. So if a perturbation changes the phase of the oscillator, there is no "restoring force" and the phase error persists.

Also, the output spectrum has bands around w_0 and its harmonics, as it is shown on the following Figure 4.18. With the increasing order of the harmonics of w_0 the power in the side bands is decreased [13].

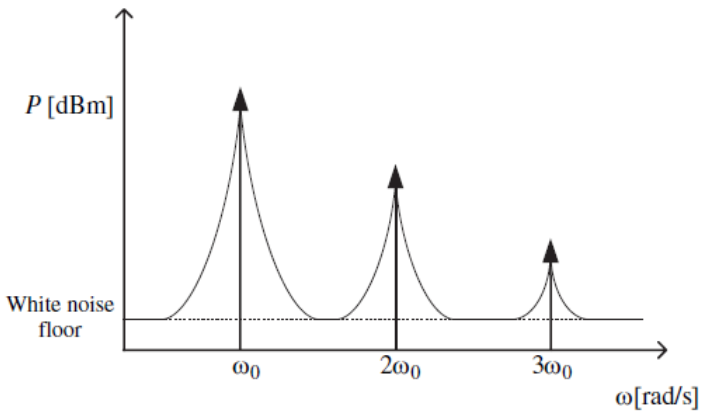


Figure 4.18: Spectrum of oscillator output [16]

The noise can be generated either inside the circuit (due to active and passive devices) or outside (e.g., power supply). Effects such as non-linearity and periodic variation of circuit parameters are very important while designing an oscillator and make it very

difficult to predict phase-noise. This noise causes fluctuations of both amplitude and phase. In practical oscillators there is an amplitude stabilization scheme, which attenuates amplitude variations, phase-noise is usually dominant. The oscillator noise can be characterized either in the frequency domain (phase-noise), or in the time domain (jitter). Phase-noise is used by analog and RF designers, and jitter is used by digital designers. There are many ways to quantify these fluctuations of phase and amplitude in oscillators. They are often characterized in terms of the single side band noise spectral density, $\mathcal{L}(w_m)$, expressed in decibels below the carrier per hertz (dBc/Hz). This characterization is valid for all types of oscillators and is defined as:

$$\mathcal{L}(w_m) = \frac{P(w_m)}{P(w_0)} \tag{4.26}$$

where $P(w_m)$ is the single sideband noise power at a "distance"of w_m from the carrier (w_0) in a 1 Hz bandwidth and $P(w_0)$ is the carrier power.

The advantage of this parameter as a guiding line is its ease of measurement. This can be done by using a spectrum analyzer (introduces errors) or dedicated (and expensive) equipment such as phase or frequency demodulators, well characterized and with well known properties. Note that the spectral density includes both phase and amplitude noise, and they can not be separated. However, practical oscillators have an amplitude stabilization mechanism, which strongly reduces the amplitude noise, while the phase-noise is unaffected. Thus, the previous equation ($\mathcal{L}(w_m)$) is dominated by the phase-noise and it is known simply as “phase-noise”. The carrier-to-noise ratio, CNR, can also be used to specify the oscillator phase noise. The CNR in a 1 Hz frequency band at the distance of w_m from the carrier w_0, is defined as [16]:

$$CNR(w_m) = \frac{1}{\mathcal{L}(w_m)}. \tag{4.27}$$

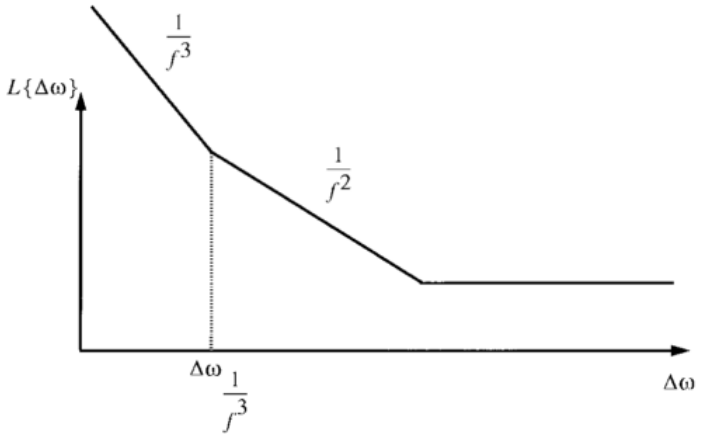


Figure 4.19: Typical plot of the phase noise of an oscillator versus offset from carrier [13]

It is customary to characterize an oscillator in terms of its single-sideband phase noise as it is shown in the previous figure. Therefore, taking a closer look into the carrier

graphic where the phase noise in dBc/Hz is plotted as a function of angular frequency offset, $\Delta\omega$, with the frequency axis on a log scale, the relative power at an offset frequency $\Delta\omega$ from the carrier drops very rapidly.

Note the actual curve is approximated by a number of regions, each having a slope of $1/f^x$, where $x = 0$ corresponds to the "white"phase noise region (slope = 0 dB/decade), and x = 1, corresponds to the "flicker"phase noise region (slope = ˇ$20dB/decade$). There is clearly a region where the slope is $20dB/dec$. But this range only holds until the noise flattens out. Also, very near the carrier, the slope increases to approximately $30dB/dec$. There are also regions where $x = 4, 5$, and these regions occur progressively closer to the carrier frequency [13].

4.4.1.1 Leeson-Cutler Phase Noise Model

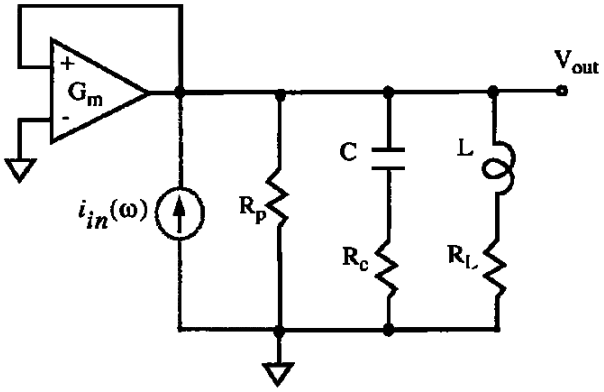


Figure 4.20: A typical RLC oscillator [6]

The model known as Leeson-Cutler phase noise model is based on a linear time invariant assumption for tuned tank oscillators, such as the one represented in Figure 4.20. It predicts the following behavior [6]:

$$\mathcal{L}_{total}\{\Delta\omega\} = 10log\left\{\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{4.28}$$

where F is an empirical parameter often called "device excess noise number", k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_o is the oscillation frequency, Q_L is the effective quality factor of the tank with all the loadings in place (also known as loaded Q), $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f^3}$ is the frequency of the corner between $1/f^3$ and $1/f^2$ regions, as shown in the sideband spectrum of the Figure 4.19 [6].

4.4.2 Jitter

The signals at the input and output of a PLL are often squared waves representing binary signals, as are many of the signals within the PLL. The noise on binary signals is commonly characterized in terms of jitter [10].

Jitter is a random and an undesired perturbation or uncertainty in the timing of events. Usually, the events of interest are the transitions in a signal. Jitter can be modeled as a noise-free signal v and a displacing time with a stochastic process j. The noisy signal becomes

$$v_n(t) = v(t + j(t)) \tag{4.29}$$

with j assumed to be a zero-mean process and v assumed to be a T-periodic function. j has units of seconds and can be interpreted as a noise in time. Alternatively, it can be reformulated as a noise is phase, or phase noise, using

$$\phi(t) = 2\pi f_o j(t) \tag{4.30}$$

where $f_o = 1/T$ and

$$v_n(t) = v\left(t + \frac{\phi(t)}{2\pi f_o}\right). \tag{4.31}$$

4.4.2.1 Jitter Metrics

Defining t_i as the sequence of times for positive-going threshold crossings, previously referred to as transitions, that occur in v_n. Various jitter metrics characterize the statistics of this sequence. The simplest metric is the edge-to-edge jitter, J_{ee}, which is the variation in the delay between a triggering event and a response event [10]. When measuring edge-to-edge jitter, a clean jitter-free input is assumed, and so the edge-to-edge jitter J_{ee} is defined as

$$J_{ee}(i) = \sqrt{var(t_i)} \tag{4.32}$$

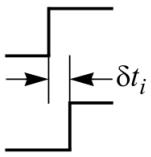


Figure 4.21: Edge-To-Edge Jitter [10]

Edge-to-edge jitter assumes an input signal, and so is only defined for driven systems. It is an input-referred jitter metric, meaning that the jitter measurement is referenced to a point on a noise-free input signal, so the reference point is fixed. This kind of signal does not exist in autonomous systems [10].

The remaining jitter metrics are suitable for both driven and autonomous systems. They gain this generality by being self-referred, meaning that the reference point is on

the noisy signal for which the jitter is being measured. These metrics are usually more complicated because the reference point is noisy, which acts to increase the measured jitter.

Edge-to-edge jitter is also a scalar jitter metric, and it does not transmit any information about the correlation of the jitter between transitions.

The next metric characterizes the correlations between transitions as a function of how far they are separated in time [10].

Defining $J_k(i)$ to be the standard deviation of $t_{i+k} - t$,

$$J_k(i) = \sqrt{var(t_{i+k} - t)} \quad (4.33)$$

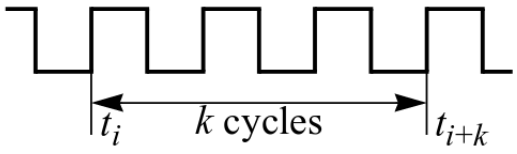


Figure 4.22: k-cycle jitter [10]

$J_k(i)$ is refered to as k-cycle jitter. It's a measure of the uncertainty in the length of k cycles and has units of time.

J_1, the standard deviation of the length of a single period, is often referred to as the period jitter, and it denoted J, where $J = J_1$ [10].

Another important jitter metric is cycle-to-cycle jitter. Defining $T_i = t_{i+1} - t_i$ to be the period of cycle i. Then the cycle-to-cycle jitter J_{cc} is

$$J_{cc}(i) = \sqrt{var(T_{i+1} - T_i)} \quad (4.34)$$

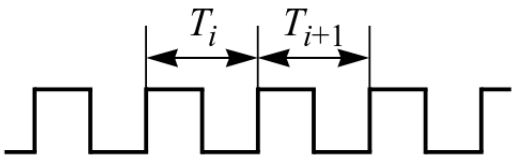


Figure 4.23: Cycle-to-cycle Jitter [10]

Cycle-to-cycle jitter is a metric designed to identify large adjacent cycle displacements. It is similar to the edge-to-edge jitter metric in the sense that it is a scalar jitter metric that does not contain information about the correlation in jitter between distant transitions. However, it differs in that it is a measure of short-term jitter that is relatively insensitive to long-term jitter. As such, cycle-to-cycle jitter is the only jitter metric that is suitable for use when flicker noise is present. All other metrics are unbounded in the presence of flicker noise.

If $j(t)$ is either stationary or T-cyclostationary, then t_i is stationary, meaning that these metrics do not vary with i, therefore $J_{ee}(i)$, $J_k(i)$, and $J_{cc}(i)$ can be shortened to J_{ee}, J_k, and J_{cc} [10].

CHAPTER 5

PLL Blocks

5.1 VCO

A Voltage Controlled Oscillator (VCO) is a non-linear device (oscillator) that can be tuned over a certain frequency range by varying its supply voltage [2].

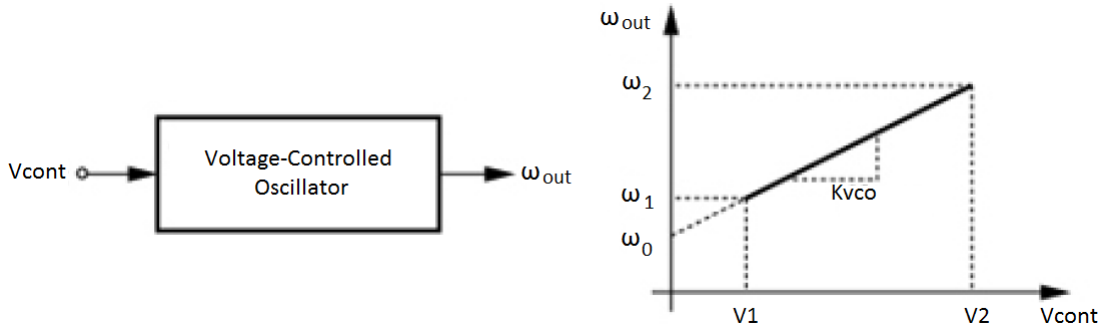


Figure 5.1: VCO characteristic [23]

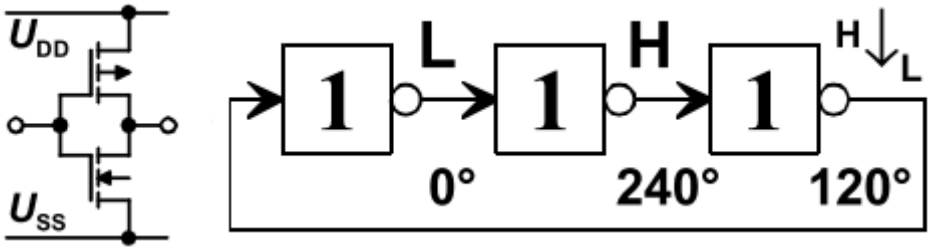
Figure 5.1 shows the desired behaviour of a VCO. Depending on V_{cont} (varying between V_1 and V_2) the output frequency will be different (between ω_1 and ω_2). The gain (or sensitivity) of the VCO is called K_{VCO} [23], which can be obtained by calculating the slope of the characteristic curve:

$$K_{VCO} = \frac{\partial \omega}{\partial V} \left[\frac{rad/s}{V} \right]. \tag{5.1}$$

K_{VCO} directly influences the tunning range and the phase noise. With a low K_{VCO} it is possible to achieve low power supply sensitivity which means a low PLL jitter, but results in a small tuning range.

5.1.1 Previously Oscillators Studies

5.1.1.1 Single Ended Ring Oscillator



a Inverter b 3-stage single ended ring oscillator

Figure 5.2: Single ended ring oscillator [24]

The previous Figure 5.2b shows a basic single ended ring oscillator. It is composed by three inverters, depicted in 5.2a in series, and the last one's output is connected to the first one's input, forming a loop. To determine the frequency at which this circuit will oscillate, it is assumed that the delay through each inverter is τ (in seconds). The signal must go through N inverters, each with delay τ, for a total time of $N\tau$, to obtain the first π phase shift. Then, the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2N\pi$. As it is known, the frequency is the reciprocal of the period, resulting in the the following equation for f_{osc}:

$$f_{osc} = \frac{1}{2N\tau_{inverter}} \tag{5.2}$$

There are many advantages of using CMOS-based technology on designing Ring Oscillators, and they are:

- Easy to design;
- Have a small and simple layout;
- Can achieve oscillation state at low voltage;
- Can achieve high oscillation frequency with low power dissipation;
- Can be electrically tuned with a wide tuning range;
- Have rail-to-rail voltage swing;
- Are compatible with digital circuitry;

- Can be used with multiphase outputs, due to their basic structure. The outputs can be logically combined to make multiphase clock signals, which have considerable uses in applications on communication systems [11].

Wide voltage tuning range of ring oscillators are particularly attractive for PLL based frequency synthesis and clock signal generation required by many applications like frequency synthesizer and data clock recovery circuits for serial data communication. The ring oscillator is the most widely manufactured integrated circuit of all. Foundries use ring oscillators on every semiconductor wafer to monitor the gate delay and speed-power product of fabricated CMOS inverters [1].

5.1.1.2 Quadrature Ring Oscillator

A single-ended VCO such as that in 5.1.1.1 suffers from a large problem in that it is susceptible to common-mode noise. To alleviate this problem, many VCOs use a differential delay stage. Also note that a VCO using differential delay stages can have an even number of stages if the feedback lines are swapped.

The same principle can be applied on single-ended ring oscillators, but by having two outputs that have a 180 degree shift, therefore having a quadrature ring oscillator.

For quadrature outputs, a ring with an even number of inverter stages is required. An even number of stages has a stable and static operating point("latch-up") and, therefore, does not oscillate. One method to solve this issue consists in adding feed-forward inverters between nodes with opposite-phase signals, as shown in Figure 5.3, a pair can operate as a negative-Gm cell or as regenerative circuit [24].

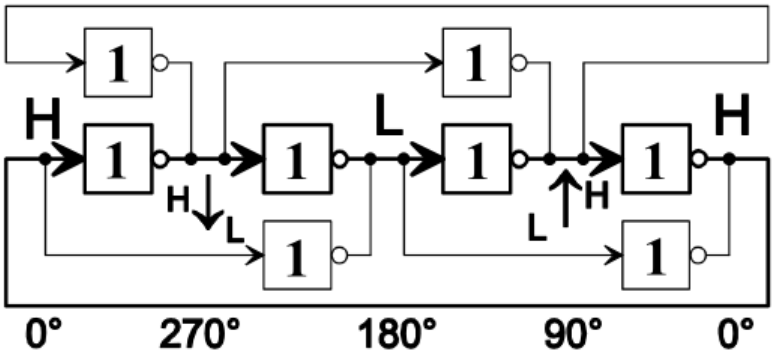


Figure 5.3: Quadrature ring oscillator [24]

Since the transition does not have to travel twice in the ring, the oscillation frequency is given by

$$f_{osc} = \frac{1}{N\tau_{inverter}} \tag{5.3}$$

where, again, N is the number of inverter stages and τ is the delay of an inverter stage.

5.2 Frequency Dividers

A frequency divider (also called clock divider, scaler or pre-scaler), is a circuit that takes an input signal of a frequency, f_{in}, and generates an output signal of a frequency given by:

$$f_{out} = \frac{f_{in}}{N} \tag{5.4}$$

where N is an integer [28].

Frequency dividers are widely used in PLL and frequency synthesizers in order to generate a frequency that is a multiple of the reference frequency. These frequency dividers can also be implemented for both analog and digital applications [28].

Analog frequency dividers are less common and are usually used at very high frequencies. Digital dividers implemented in modern IC technologies can work up to tens of GHz [28].

In the next subsections, a brief explanation of both analog and digital frequency dividers as well as some different techniques applied on both cases are presented, for different uses. The focus will be on simple implementations instead of a large variety of implementations.

5.2.1 Regenerative Frequency Divider

A regenerative frequency divider, also known as Miller Frequency Divider, mixes the input signal with the feedback signal coming from the mixer [28].

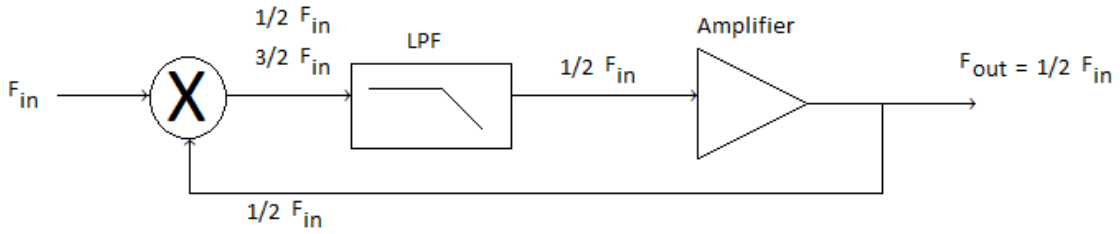


Figure 5.4: Regenerative Frequency Divider

As it can be seen in the previous figure, the feedback signal is $\frac{1}{2}f_{in}$. This system produces sum and difference frequencies $\frac{1}{2}f_{in}$ and $\frac{3}{2}f_{in}$ at the output of the mixer. A low pass filter removes the higher frequency and the $\frac{1}{2}f_{in}$ frequency is amplified and fed back into mixer [28].

5.2.2 Digital Divider

For power-of-2 integer division, a simple binary counter can be used, clocked by the input signal. The least-significant output bit alternates at $\frac{1}{2}$ the rate of the input clock, the next bit at $\frac{1}{4}$ the rate, the third bit at $\frac{1}{8}$ the rate, etc., as it can be seen on 5.5. An arrangement

of D flip-flops is a classic method for integer-n division. Such division is frequency and phase coherent to the source over environmental variations including temperature. The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of three of these, such system would be a divide-by-8. By adding additional logic gates to the chain of flip flops, other division ratios can be obtained. Integrated circuit logic families can provide a single chip solution for some common division ratios [28].

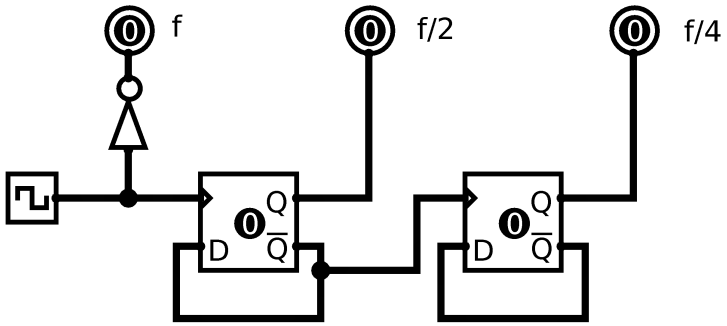


Figure 5.5: Flip-Flop D based Frequency Divider [28]

5.2.3 Fractional-N Divider

A fractional-N frequency synthesizer can be constructed using two integer dividers, a divide-by-N and a divide-by-$(N+1)$ frequency divider. With a modulus controller, N is toggled between the two values so that the VCO alternates between one locked frequency and the other. The VCO stabilizes at a certain frequency that is the time average of the two locked frequencies. By varying the percentage of time the frequency divider spends at the two divider values, the frequency of the locked VCO can be selected with very fine granularity [28].

5.2.3.1 Delta-Sigma Fractional-N Divider

If the sequence of divide by N and divide by $(N+1)$ is periodic, spurious signals appear at the VCO output in addition to the desired frequency. Delta-sigma fractional-n dividers overcome this problem by randomizing the selection of N and $(N+1)$, while maintaining the time-averaged ratios [28].

5.2.4 Synchronous vs Asynchronus Dividers and Advantages of using Asynchronous Divider

There are two kinds of dividers, synchronous and asynchronous.

A synchronous circuit is governed by a global clock signal generated by an oscillator. The state of all elements of a synchronous circuit changes only by an application of a distributed clock signal. So, this makes the state of a synchronous circuit predictable. Also, synchronous clock signals are less susceptible to noise, circuit anomalies and hence

safer to design and operate. But they are limited in operation of speed by the propagation delay of the clock signal in reaching all the elements of the clock signal. The time period of a clock signal should be long enough to accommodate longest propagation delay. Practically all the circuits today are synchronous circuits, except the where speed of the circuit operation is crucial.

In other hand, an asynchronous circuit changes its state only through the inputs received by them. So, the operation is quite instantaneous since they don't have to wait for a clock pulse. They are limited by propagation delay of logic gates only. But asynchronous circuits can transition into a wrong state due to incorrect arrival time of 2 inputs. This is called a race condition. Asynchronous circuits are considered quite difficult to design for a reliable operation. These are used primarily in high speed systems such as Signal Processing hardware [27].

There are pros and cons on using asynchronous dividers, an these are:

Table 5.1: Pros and cons of using an asynchronous divider [17, 27]

Pros	Cons
Fast and of simple implementation	
Occupy small area	Have long latency for large dividers
Each stage runs at lower frequency	Divide by a multiple of two only
Reduced power consumption	Jitter accumulation
Reduced high frequency clock loading	

However, they can be used as front end to synchronous counter divider to reduce speed requirements [27].

5.2.5 Previous Divider Studies

5.2.5.1 Master-Slave 1/2 Divider

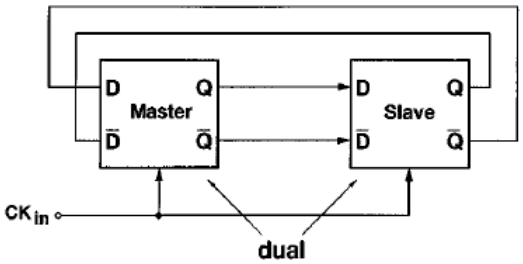


Figure 5.6: Master-Slave Latch D Divider with single Clock[22]

The 1/2 frequency divider employs two D-latches in a master-slave configuration with negative feedback. In high speed master-slave dividers, it is common practice to design the slave as the "dual" of the master, as it can be seen on 5.6 so that they can be both driven by a single clock [22].

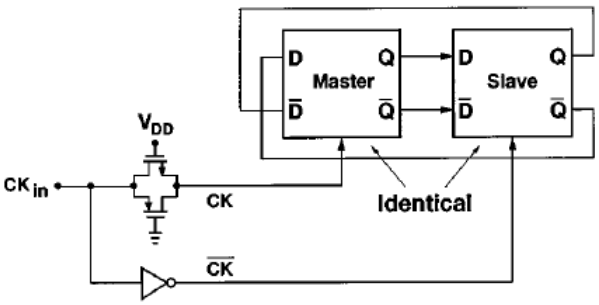


Figure 5.7: Master-Slave Latch D Divider with Complementary Clocks[22]

However, duality requires one of the latches to incorporate PMOS devices in the signal path, therefore lowering the maximum speed. To avoid this difficulty, as shown in 5.7, the divider uses two identical D-latches that are driven by complementary clocks CK and $\overline{CK}$. In order to minimize the skew between CK and $\overline{CK}$, the non-inverted phase is delayed by means of a complementary pass gate having devices identical with those in the master. It is known that skew increases as the input transition time becomes comparable with the period [22]. Also, this problem can be surpassed if complementary clock signals are used (from a differential VCO, for example).

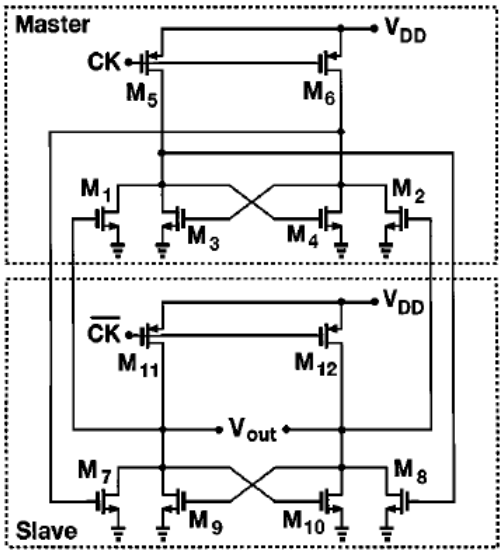
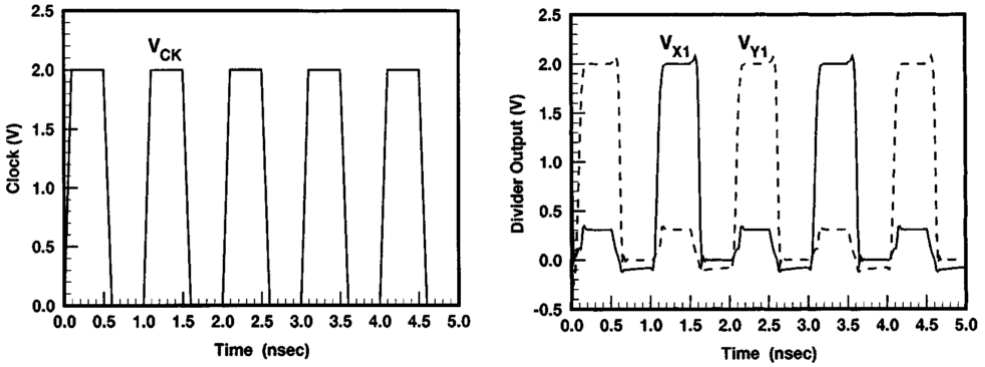


Figure 5.8: Divider Circuit[22]

Circuit Figure 5.8 depicts the divider circuit. Each latch consists of two sense devices (M_1 and M_2 in the master and M_7 and M_8 in the slave), a regenerative loop (M_3 and M_4 in the master and M_9 and M_{10} in the slave), and two pull-up devices (M_5 and M_6 in the master and M_{11} and M_{12} in the slave). When $CK$is high, M_5 and M_6 are off and the master is in the sense mode, while M_{11} and M_{12} are on and the slave is in the store mode. When CK goes low, the reverse occurs. Note that the circuit uses no stacked or pass transistors. Also, the gate channel capacitance of the PMOS transistors hardly affects the critical path

because these devices are (velocity) saturated almost for the entire voltage swing at the output. In contrast with conventional latch topologies, the D-latch circuit used in this divider does not disable its input devices when it goes from the sense mode to the store mode. While this would pose timing problems in a general digital circuit, it does not prevent the divider from functioning properly. To explain the reason, two observations are made. First, since the input devices of each latch are N-type, they can change the state only if one of the inputs goes from low to high (and the other from high to low). Second, when each latch is in the sense mode, neither of its outputs can go from low to high because the PMOS pull-up devices are off. Thus, if, for example, the master is in the sense mode and the slave in the store mode, the master's outputs can only go from high to low and hence cannot override the state stored in the slave [22].

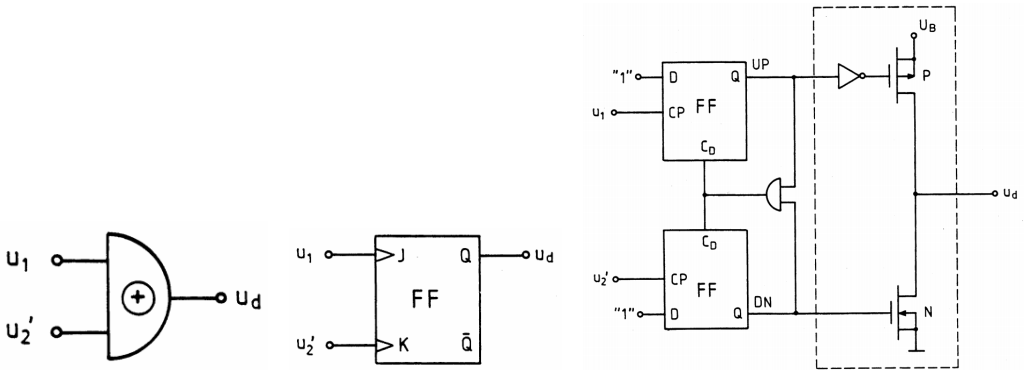


a Divider Input Signal b Divider Output Signal

Figure 5.9: Divider Input and Output Signals [22]

5.3 Phase-Frequency Detector and Charge Pump

In this kind of PLL, a number of different logical circuits can be used as a phase detector. The three more used and more important are represented in the following Figure 5.10:



a EXOR gate [3] b JK Flipflop [3] c Phase-Frequency Detector [3]

Figure 5.10: Phase detectors [3]

5.3.1 EXOR gate

This type of detector is most similar to the previously mentioned linear multiplier. The signals in DPLLs are always binary signals, i.e., square waves. It is assumed that the signals u_1 and u_2' are symmetrical square waves. The following figure depicts the waveforms of the EXOR phase detector for different phase errors θ_e [3].

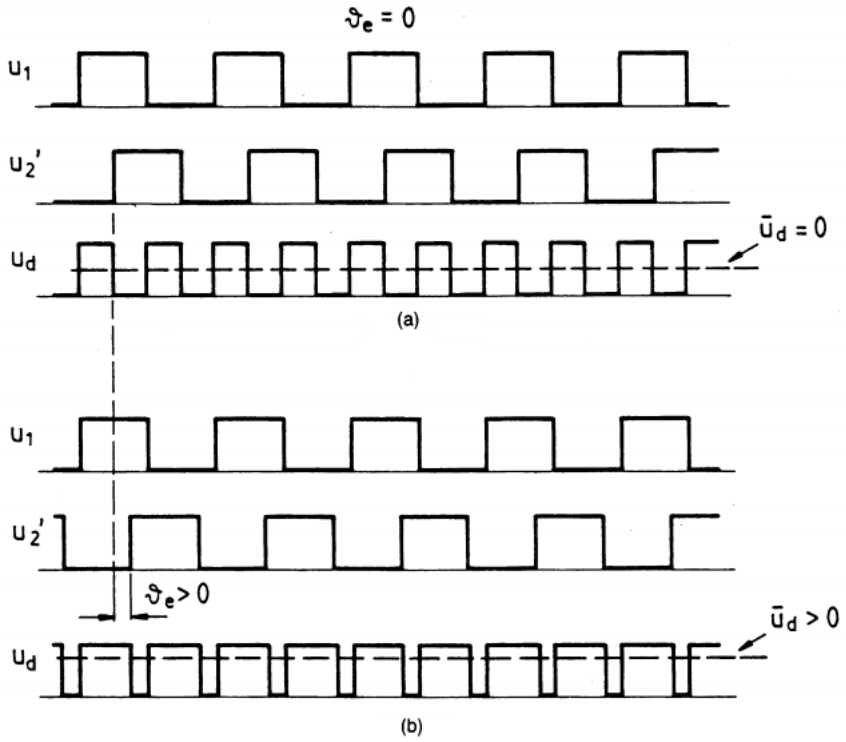


Figure 5.11: Waveforms of the signals for the EXOR phase detector
a) Waveforms at zero phase error ($\theta_e = 0$)
b) Waveforms at positive phase error ($\theta_e > 0$) [3]

At zero phase error, the signals u_1 and u_2' are out of phase by exactly 90°as show in Figure 5.11(a). The output signal u_d is a square wave with twice the frequency of the reference signal, therefore the duty cycle of u_d is half of u_1 [3].

Due to the filtering process of the high frequency components, only the average value of u_d is taken in account, therefore is represented by $\overline{u_d}$ in the previous Figure 5.11. This value is the arithmetic mean of the two logical levels. In the first case when it is considered that the average value is zero and it is considered that this value is the quiescent point of the EXOR. In the second case, 5.11(b), if the output signal u_2' lags the reference signal u_1, it os possible to verify that the phase error θ_e becomes positive. Therefore the duty cycle of u_d becomes larger than a half of u_1 and the average value u_d' becomes greater than 0 [3].

If u_d' reaches its maximum value, it corresponds to a phase error of $\theta_e = 90°$; if u_d' reaches its minimum value, it corresponds to a phase error of $\theta_e = -90°$ [3]. Plotting u_d' vs θ_e gets the following Figure 5.12(a). Whereas the output signal of the four-quadrant

multiplier varies with the sine of phase error, u_d' of the EXOR is a triangular function of phase error. Within a phase error range of $-\pi/2 < \theta_e < \pi/2$, u_d is proportional to θ_e and it can be written as

$$\overline{u_d} = K_d \theta_e. \tag{5.5}$$

In the EXOR phase detector case, the phase detector gain K_d is constant. If, for example, the supply voltage is V_{dd} and V_{ss} (therefore the logic levels correspond to V_{dd} and V_{ss}), the gain K_d can be described as

$$K_d = \frac{V_{dd} - V_{ss}}{\pi}. \tag{5.6}$$

If the output signal of the EXOR has some saturation at higher or lower value, it can also be expressed as

$$K_d = \frac{V_{sat}^{+} - V_{sat}^{-}}{\pi}. \tag{5.7}$$

In similarity with the four-quadrant multiplier, the EXOR phase detector can maintain phase tracking when the phase error is maintained in the same range of

$$-\pi/2 < \theta_e < \pi/2. \tag{5.8}$$

The performance of the EXOR phase detector is affected when the signals u_1 and u_2' are asymmetrical. When such happens, the output signal $\overline{u_d}$ gets clipped at some intermediate level and it reduces the loop gain of the DPLL, resulting in a smaller lock range, shown in Figure 5.12(b) [3].

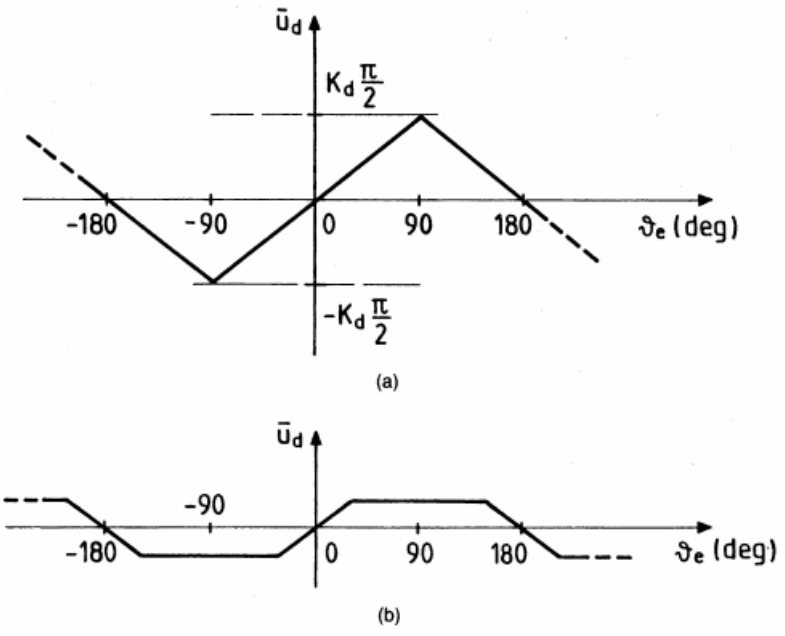


Figure 5.12: Plot of $\overline{u_d}$ vs phase error θ_e
a) Normal case: waveforms u_1 and u_2' in Figure 5.11 are symetrical waves
b) Waveforms u_1 and u_2' in Figure 5.11 are asymmetrical. The characteristic of the phase detector is clipped [3]

Although in EXOR-based the waveform symmetry is important, it is not in the next phase detector, the JK Flipflop, as it will be shown in 5.3.2.

5.3.2 JK Flipflop

The JK Flipflop is also used in phase detection for PLLs. This kind of JK is different from usual because it's edge-triggered. A positive edge at the input J (u_1) triggers the output u_d to the logic "high"state (Q=1), whereas a positive edge at the input K (u_2') triggers the output u_d to the logic "low"state (Q=0). Without phase error u_1 and u_2' have opposite phase. The output signal u_d represents a symmetrical square wave whose frequency is identical to the reference frequency. In this case, it is considered that the average value of u_d ($\overline{u_d}$) is zero, therefore the phase error is also zero ($theta_e$=0) [3]. This can be seen in the following Figure 5.13(a).

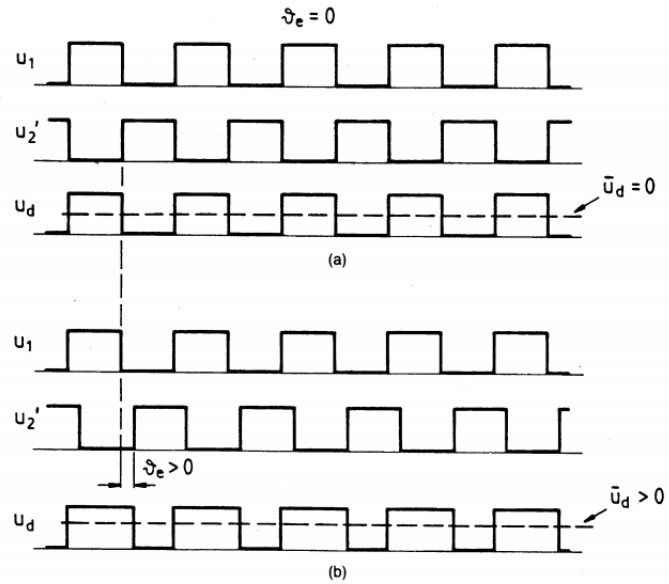


Figure 5.13: Waveforms of the signals for the JK Flipflop-based phase detector
a) Waveforms at zero phase error ($\theta_e = 0$)
b) Waveforms at positive phase error ($\theta_e > 0$) [3]

If the phase error becomes positive, as shown in Figure 5.13(b), the duty cycle of the u_d signal is greater than a half, therefore $\overline{u_d}$ is positive. It can be seen that u_d is at its maximum value when the phase error reaches 180°and reaches its minimum value when the phase error reaches -180°[3].

The characteristic curve for $\overline{u_d}$ vs. phase error θ_e is demonstrated in the following Figure 5.14. Within the range of $-\pi < \theta_e < \pi$, $\overline{u_d}$ is proportional to θ_e and it's given by

$$\overline{u_d} = K_d \theta_e. \tag{5.9}$$

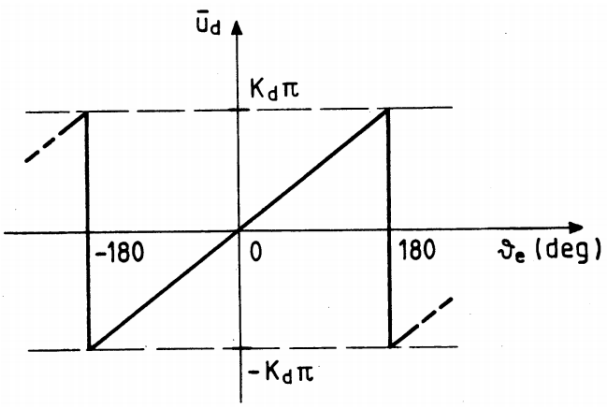


Figure 5.14: Plot of u'_d vs phase error θ_e [3]

Also, it can be seen by the previous Figure 5.14 is able to maintain phase tracking error in the range

$$-\pi < \theta_e < \pi. \tag{5.10}$$

Considering that the supply for JK Flipflop is V_{dd} and V_{ss}), its gain can be given as

$$K_d = \frac{V_{dd} - V_{ss}}{2\pi} \tag{5.11}$$

and if saturation is considered, it can be given as

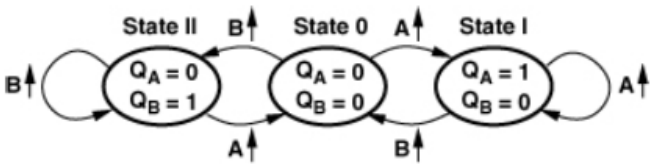
$$K_d = \frac{V_{sat}^{+} - V_{sat}^{-}}{2\pi}. \tag{5.12}$$

As stated before, the symmetry of the signals u_1 and u'_2 is irrelevant due to the JK operational method: it reacts to positive transitions of these signals. Comparing with the EXOR-based phase detector, in all other aspects, these two phase detectors they have the same behavior. Due to the pull-in effect, these kind or detectors are not usually used [3]. Instead, a Phase-Frequency Detector is used.

5.3.3 Phase-Frequency Detector

A phase-frequency detector (PFD), as the name implies, is a device that compares the phase and frequency of two input signals. It has two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and another from some external source. This kind of approach depends not only on the phase error θ_e but also on frequency error $\Delta\omega = \omega_1 - \omega'_2$ when the DPLL has not yet acquired lock. It has two outputs, usually named as "Up"and "Down"which instruct subsequent circuitry on how to adjust to lock onto the phase and frequency.

To form a PLL, the PFD phase error output is fed to a loop filter which integrates the signal to smooth it. This smoothed signal is fed to a voltage-controlled oscillator which generates an output signal with a frequency that is proportional to the input voltage. The VCO output is also fed back to the PFD to form the PLL circuit [21].



a Desired PFD state diagram

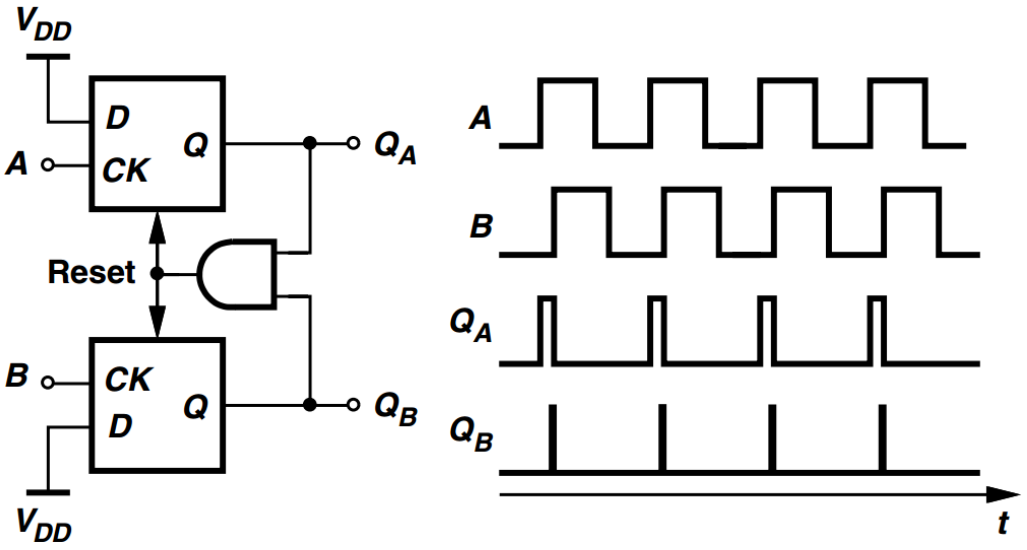
Up	Down	Result
0	0	No Change
0	1	Go Slower
1	0	Go Faster
1	1	Avoid Dead Zone

b Desired PFD state diagram table

Figure 5.15: Desired PFD states [4]

Figure 5.15a illustrates the desired state diagram of a PFD. Starting on state 0, if there is a rising edge on input A, the PFD will jump to state 1 with the output Q_A high, on the rising edge of the input B the PFD will return to state 0. The circuit works equivalently if the first rising edge happens on input B [4].

The logical implementation is shown in Figure 5.16a. It consists of two edge-triggered, resettable flip-flop D with the D input connected to VDD (logical '1'). A and B act as the flip flops clock signal. When $Q_A = 1$, $Q_B = 1$, the AND gate resets both flip-flops [4].



a PFD logical implementation

b PFD output diagram example

Figure 5.16: Phase-Frequency Detector [4]

Note that the effect of reset pulses on Q_B do not interfere with the operation since only the average value of $Q_A - Q_B$ is of interest, however they introduce a number of errors that influence the ripple on the control voltage [4].

5.3.4 Charge Pump

The purpose of a charge pump is basically converting phase errors from the PFD (digital domain) into charge (current, in analogical domain). A charge pump sinks or sources current during a period of time. In the example shown in Figure 5.17, assuming that a pulse of width ΔT turns S_1 on and I_1 charges C_1, V_{out} increases by an amount equal to

$\Delta T \cdot \frac{I_1}{C_1}$. Correspondingly, a pulse on S_2 results a drop in V_{out}. Should Up and Down be active simultaneously, I_1 will simply flow through S_1 and S_2 to I_2 causing no change in V_{out} [4].

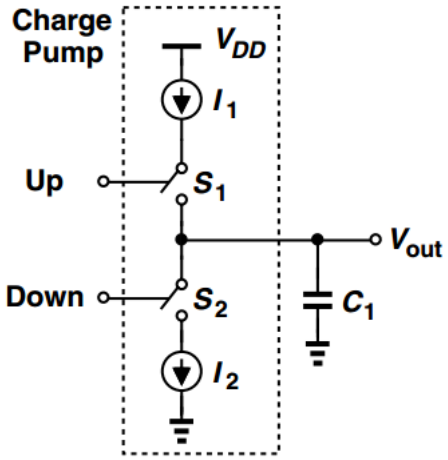
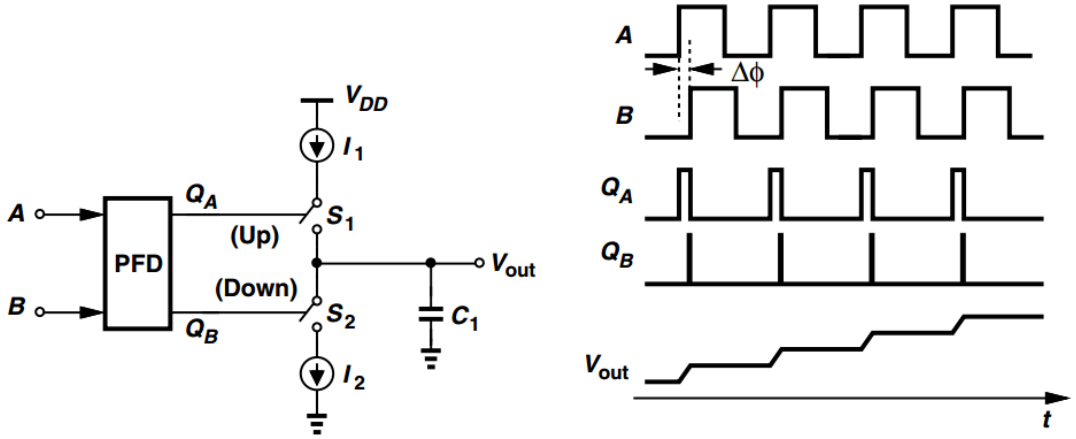


Figure 5.17: Charge Pump [4]

Combining the charge pump with the PFD shown in Figure 5.16, as shown in the figure below, yields a circuit that displays the behaviour of an integrator.If, for example, A leads B, Q_A produces pulses, consequently charging C_1 and slowly driving V_{out} to $+\infty$ [4].



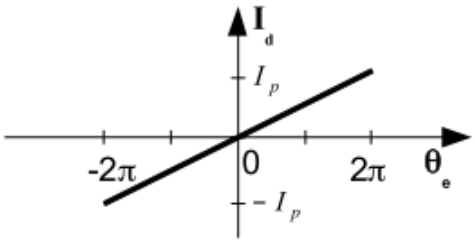
a PFD-CP implementation

b PFD-CP output representation

Figure 5.18: Phase-Frequency Detector [4]

In other words, if the phase difference is constant (loop is locked) this circuit produces a ramp-like response [4].

The gain, K_d, of the Charge Pump can be obtain by calculating the slope of the transfer function as shown in the next figure.



$$K_d = \frac{\partial I_D}{\partial \theta_e} = \frac{I_p}{2\pi}\left[\frac{A}{rad}\right] \tag{5.13}$$

Figure 5.19: Charge Pump Transfer Function

5.3.5 Common PFD-CP Problems

5.3.5.1 Phase Detector Dead Zone

This occurs when digital phase detectors are used. It is found that when the loop is in lock and there is a small phase difference between the two signals, very short pulses are created by the phase detector logic gates. Being very short, these pulses may not propagate and add charge into the charge pump/loop filter. As a result the loop gain and linearity is reduced and this forces up the loop jitter/phase noise.

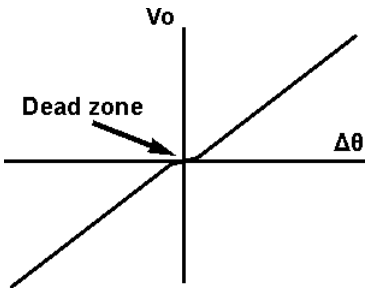
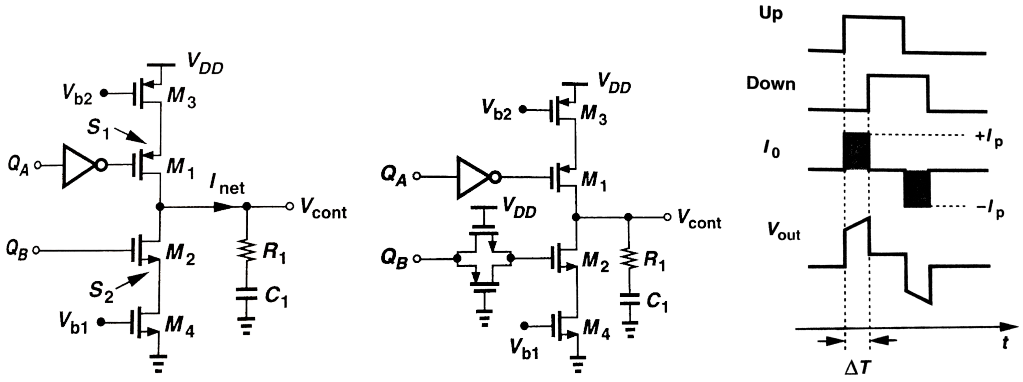


Figure 5.20: PFD Dead Zone [20]

To overcome this issue one solution is to add a delay in the phase detector reset path, between the output of the AND gate the dual D-type detector reset terminals. This forces a minimum pulse length. One common delay adding technique is introducing an even number of inverters.

5.3.5.2 Up/Down Skew Mismatch

The Skew Mismatch of the Up and Down signals occurs when both pulses from the phase detector arrive at different time to the CP. It is known that, due to duality, the "Up"switch is a PMOS transistor. Therefore, a inverter must be placed in order to activate the switch. Usually the "Down"switch is a NMOS transistor, so there is no component in the PFD-CP interface. For this reason, it is known that the signal doesn't take the same time to arrive. The visible effect is a change on the current that will flow on the loop filter. One common solution is to add a pass gate to compensate the effect of skew, as it can be seen in the following Figure 5.21 represented below:



a Skew between Up and Down pulses as result of additional in-verter

b skew compensation by adding a pass gate

c up and down waveforms showing effect of skew on the output current and voltage

Figure 5.21: Up/Down Skew [4]

The negative effects of this phenomenon is that if the current is not the same it introduces phase error, according to Figure 5.21c [4].

5.3.5.3 Transistor Coupling

It is required that the transistors that constitute the CP have minimum coupling. This helps reducing jitter [4].

5.3.5.4 Power Supply Rejection Ratio

Power Supply Rejection Ratio, or PSRR is a term used to describe the capability of an electronic circuit to suppress any power supply variations to its output signal. The PSRR of a power supply can be measured by the following equation:

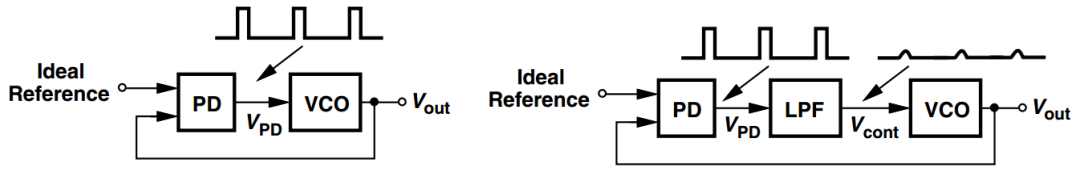
$$PSRR[dB] = 20\log_{10}\left(\frac{\Delta V_{supply}}{\Delta V_{out}}A_v\right)dB. \tag{5.14}$$

A good power supply or an insensible power supply noise charge pump in order to help on the closed loop stability [4].

5.4 Loop Filter

The PLLs' phase detector produces repetitive pulses at its output, changing the VCO frequency and generates large sidebands [4], therefore a low-pass filter (also called "loop filter") between the PD and VCO blocks to suppress the high frequency component of these pulses, as it can be seen in Figure 5.22.

There are many kinds of low-pass filters, but only the ones with completely passive components and more important approaches for this thesis are approached.



a Simple PLL b Addition of a low-pass filter and its behaviour

Figure 5.22: Simple PLL and PLL with a LPF [4]

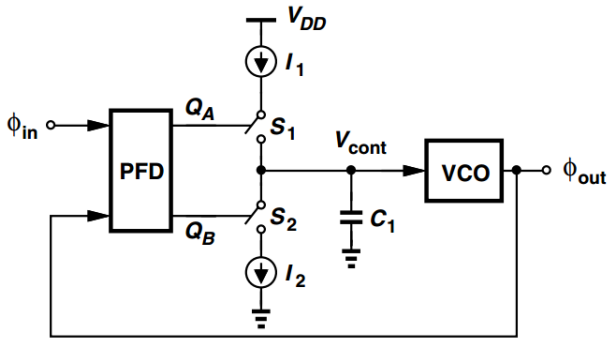


Figure 5.23: Charge-Pump PLL [4]

The first approach is a single capacitor as a filter, as shown in 5.23. This kind of design is called "Charge-Pump PLL". The C_1 capacitor is charged or discharged and drives the control voltage V_{cont} towards $+\infty$ or $-\infty$, respectively. In other words, if the PLL has the LPF circuit on 5.18a, its gain is infinite and it is defined by the final value of V_{cont} divided by the input phase difference. This leads to the PDF/CP/C_1 circuitry producing a ramp-like output response to a constant phase difference, exactly like an integrator, and its results can be seen in the following Figure 5.24 [4].

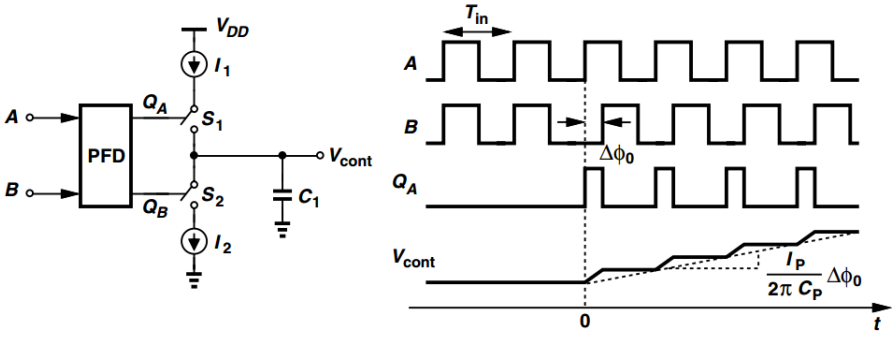


Figure 5.24: Derivation of the phase step response of the PFD/CP/C_1 cascade [4]

This happens when the phase step of $\Delta\phi_0$ at one of the PFD inputs makes the switches S_1 or S_2 turn on, therefore changing the output voltage. As it was refered before, its behavior is similar to an integrator. However, this system is not linear; if $\Delta\phi_0$ is doubled, not every point on the output waveform V_{cont} is doubled. An approximation of this waveform by a ramp is possible to do, but assuming that the charge pump constantly

charges the capacitor C_1. This is called "continuous-time (CT) approximation"and it says that the change in V_{cont} in every period is equal to

$$\Delta V_{cont} = \frac{\Delta\phi_0}{2\pi} T_{in} \frac{I_p}{C_1} \tag{5.15}$$

where $[\Delta\phi_0/(2\pi)]\,T_{in}$ is the phase difference in seconds and $I_p = I_1 = I_2$. The slope of the ramp is given by $\Delta V_{cont}/T_{in}$ and therefore

$$V_{cont}(t) = \frac{\Delta\phi_0}{2\pi} \frac{I_p}{C_1} tu(t). \tag{5.16}$$

By differentiating 5.16 in time, normalizing to $\Delta\phi_0$ and taking the Laplace transform, we have that

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_1} \frac{1}{s} \tag{5.17}$$

that works as an integrator, as predicted earlier [4].

From the equation 5.17, the closed loop transfer function for the PLL shown in Figure 5.23 is given by

$$H(s) = \frac{\frac{I_p}{2\pi C_1 s} \frac{K_{VCO}}{s}}{1 + \frac{I_p}{2\pi C_1 s} \frac{K_{VCO}}{s}} = \frac{I_p K_{VCO}}{2\pi C_1 s^2 + I_p K_{VCO}}. \tag{5.18}$$

This kind of PLL is called a type-II PLL because its transfer function has two poles at the origin. The equation 5.18 shows that in fact, there are two poles in the $j\omega$, indicating an oscillatory system. This leads to an unstable system. In order to make of these integrators "lossy", a resistor is placed in series with the capacitor. This makes the system stable [4]. The resulting circuit is shown in Figure 5.25.

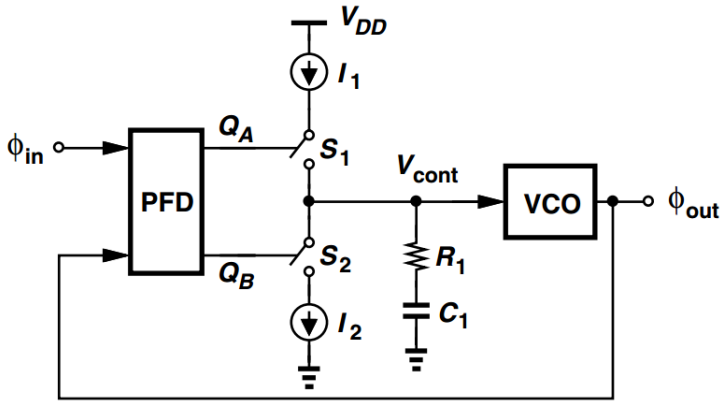


Figure 5.25: CP PLL [4]

The analysis previously made, can also be applied for this new approach. For the figure 5.25, when S_1 or S_2 turn on, V_{cont} "jumps"an amount equal to $I_p R_1$ and subsequently rises or falls linearly with time. When the switches are off, V_{cont} "jumps"in the opposite direction, resting at a voltage that is $(I_p/C_1)[\Delta\phi/(2\pi)]T_{in}$ volt higher than its value before

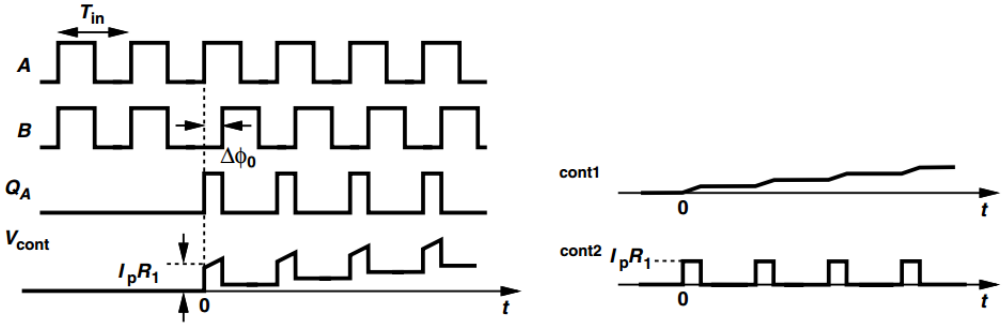
the switch operation. The resulting waveform can be viewed in Figure 5.24 as the sum of the original charge-and-hold waveform and a sequence of pulses. The area under each pulse is approximately equal to $(I_p R_1)[\Delta\phi_0/(2\pi)]T_{in}$. According to the source [4], it is possible to approximate a pulse sequence by a step of height $(I_p R_1)[\Delta\phi_0/(2\pi)]$, therefore obtaining

$$V_{cont}(t) = \frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1}tu(t) + \frac{\Delta\phi_0}{2\pi}I_p R_1 u(t). \tag{5.19}$$

The transfer function of the PFD/CP/LPF cascade is therefore given by

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{1}{C_1 s} + R_1\right) \tag{5.20}$$

therefore, the graphic obtained is depicted in Figure 5.26.



a Phase step response of PFD/CP/LPF

b Decomposition of output waveform into two

Figure 5.26: Phase step response of PFD/CP/LPF and output wave decomposition [4]

Also, the closed loop transfer function of the PLL from Figure 5.25 is given by

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi}K_{VCO}R_1 s + \frac{I_p}{2\pi C_1}K_{VCO}}. \tag{5.21}$$

As it is widely known, this is a second order system, capable of being stable.

Although this is an effort to enhance the previous approach, it isn't still adequate because does not suppress the ripple sufficiently. Supposing that the PLL is in lock condition, the Up and Down pulses arrive at different times due to PFD mismatch. By consequence, one switch is activated earlier than the other allowing its corresponding current source flow through R_1 and generates an instantaneous change of $I_p R_1$ in the control voltage. On the falling edge of Up and Down pulses, the reverse happens. Therefore, the ripple consists of positive and negative pulses of $I_p R_1$ amplitude occur every T_{in} seconds. Once that $I_p R_1$ is large it is required to reduce ripple [4].

A common solution to lower the ripple is tying a capacitor directly from the V_{cont} node to the ground. The main idea is to provide a low-impedance path for the unwanted

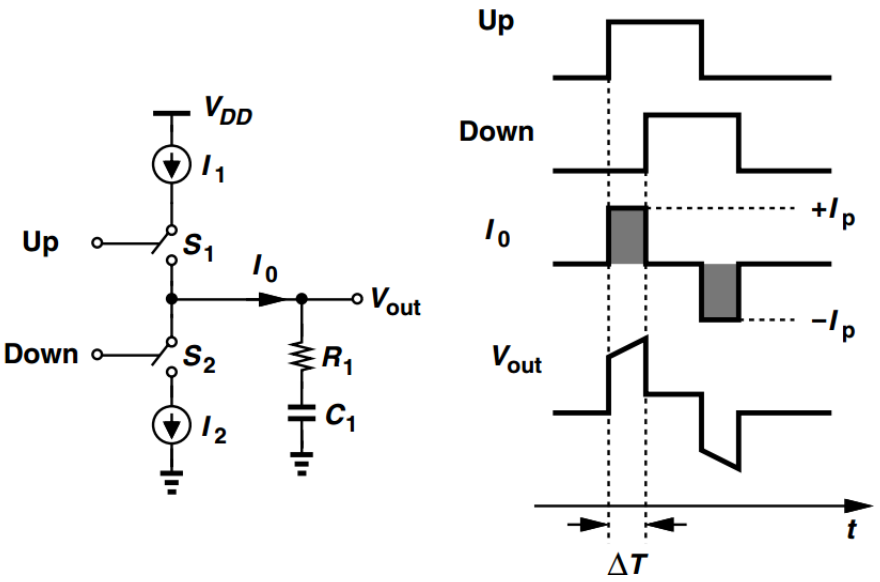


Figure 5.27: Effect of skew between Up and Down pulses [4]

charge pump output. This is, a current pulse if width ΔT produced by the CP initially flow through C_2, leading to a change of $(I_p/C_2)\Delta T$ in V_{cont}. Once that, according to the reference [4], $R_1C_2 \gg \Delta T$, the voltage change can be approximated by a ramp. After the CP turns off, C_2 shares its charge with C_1 through R_1, causing an exponential decay in V_{cont} with a time constant of R_1C_{eq} (where $C_{eq} = \frac{C_1C_2}{C_1+C_2}$). C_2 must be large enough to support a small ripple. The circuitry can be seen in Figure 5.28.

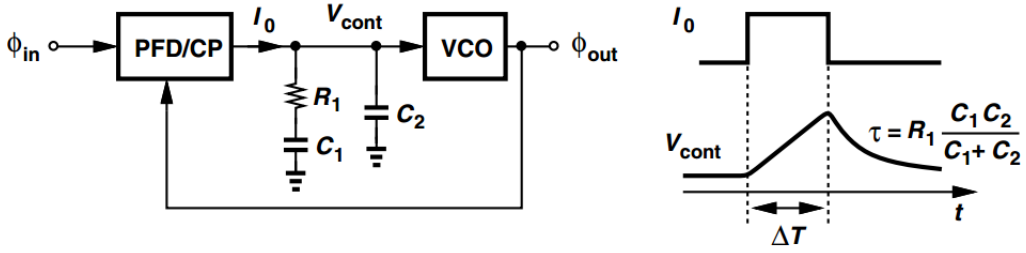


Figure 5.28: Addition of second capacitor to loop filter [4]

Another loop filter that can reduce the ripple is shown in Figure 5.29. In this situation, the ripple at node X may be large, but it is suppressed as it travels through the second low-pass filter consisting of R_2 and C_2 [4].

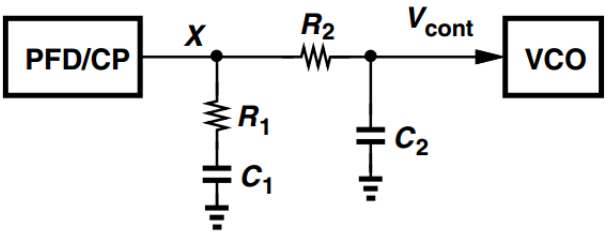


Figure 5.29: Alternative second-order loop filter [4]

Chapter 6

Block Implementation

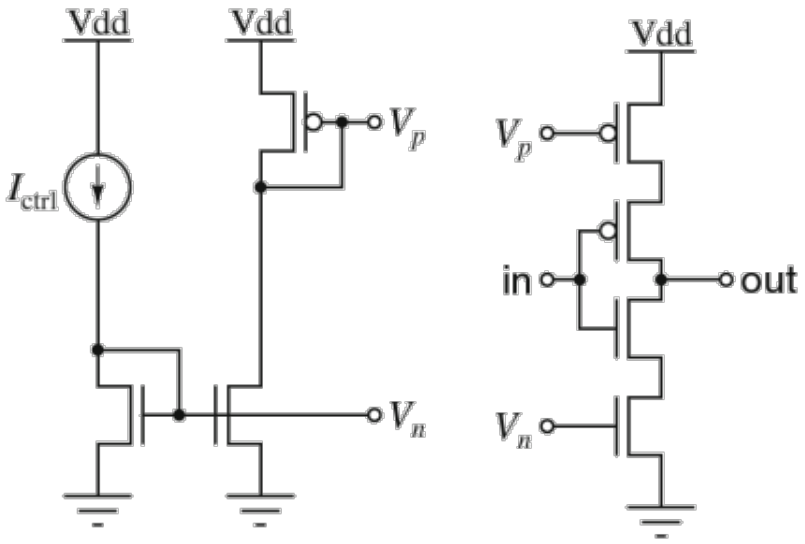
In this chapter, a brief introduction to each implemented block will be given, as well as the reason to choose each block and how it was implemented.

6.1 Implemented VCO

Starting with the VCO, a simple Current-Starved Ring Oscillator VCO is used, with the minimum power consumption and occupied area possible to fulfill the thesis requirements. It is one of the most simple way to control the oscillation frequency by changing the input voltage.

6.1.1 Current Starved Ring Oscillator

Ring oscillators can be made in many ways. The Current Starved Ring Oscillator one of them and is based in the classic ring topology but it's made by controlling the amount of current available to charge or discharge the capacitive load of each stage, therefore changing the delay of each stage. An easy way to control the current is to limit it through an adjustable current mirror through the a NMOS or PMOS transistor with the V_{ctrl} voltage input. The main components of the Current Starved Ring Oscillator are depicted in the following figure:



a Current mirror with polarization voltages b Inverter with control transistors

Figure 6.1: Current Starved Ring Oscillator components [14]

The variation of control voltage V_{ctrl} determines the frequency range and linearity of the VCO. The major drawback of this stage is longer rise/fall time when bias current is quite small because the voltage swing of the VCO becomes slower. The oscillation frequency f_{osc} is derived as follows. The total capacitance on the drains of the control transistors is given as:

$$C_{total} = C_{out} + C_{in} = C_{ox}(W_pL_p + W_nL_n) + 3/2C_{ox}(W_pL_p + W_nL_n) \tag{6.1}$$

where C_{in}, C_{out}, C_{ox} and C_{total} are the input, output, oxide related and total capacitances, respectively. The total capacitance is the sum of the output and input capacitances of the inverter and it is given by:

$$C_{total} = \frac{5}{2}C_{ox}(W_pL_p + W_nL_n). \tag{6.2}$$

The oscillation frequency is determined by the bias current, I_d, the number of stages, N, the total capacitance, C_{total} and the control voltage V_{ctrl} as:

$$f_{osc} = \frac{I_d}{2NC_{total}V_{ctrl}}. \tag{6.3}$$

In practice, a Current Starved Ring Oscillator VCO was designed and adapted to be used in a PLL. It contains the current mirrors and the inverters with control transistors as depicted in 6.1. The current mirror was modified to detect an input voltage and transform it into current, shown in Figure . It can be seen that the voltage V_{ctrl} is responsible for modulating the output frequency. The PMOS transistor controlled by this voltage works as a resistor that changes the current in the mirror. Also, note that the Bulk pin is referenced to Ground (0V); this makes transistor have less characteristic resistance,

hence making it "pass"more current, increasing the overall ring oscillator range without augmenting the other control transistors in size. Also, an inverter was placed at the output of the ring oscillator to have its output wave into a "more-squared"wave with rail-to-rail voltage, required for the next block, the divider.

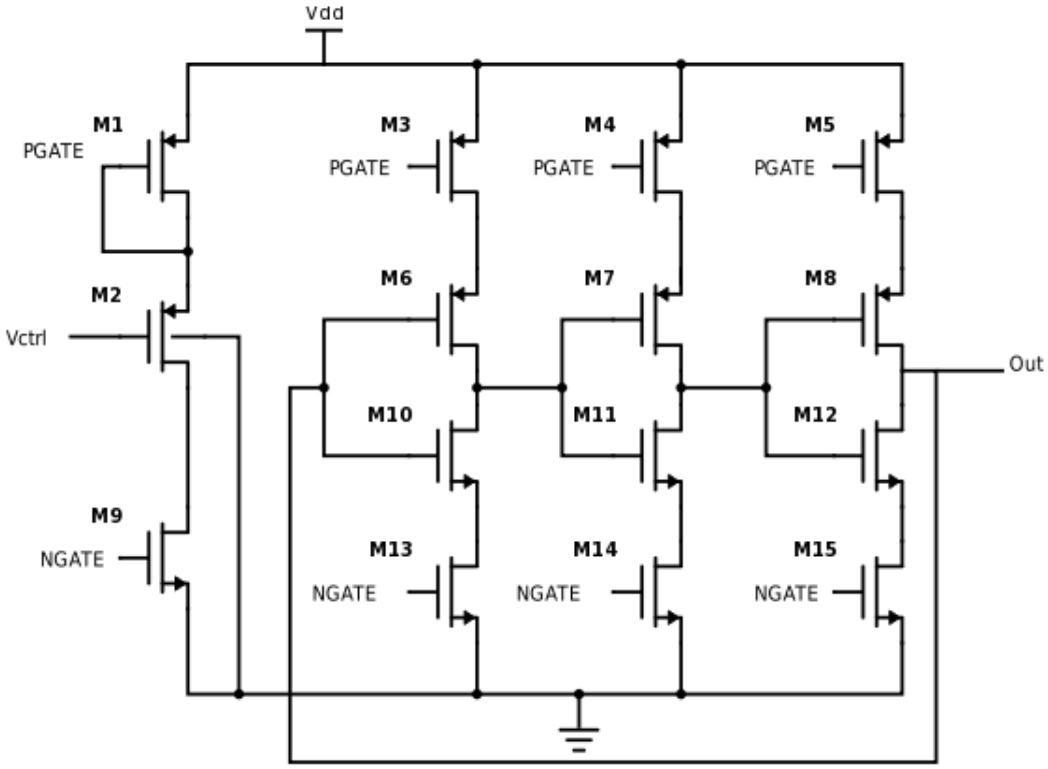


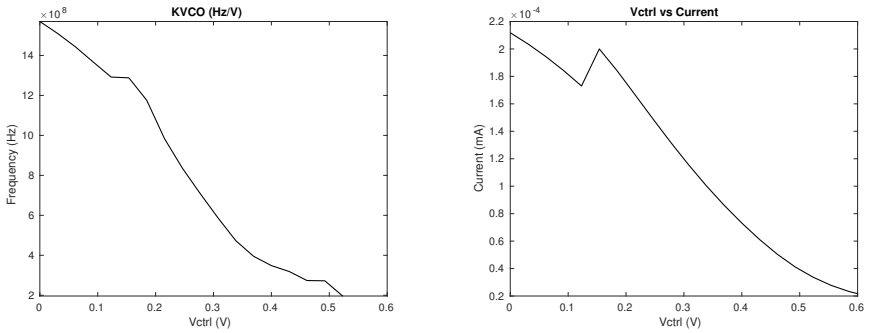
Figure 6.2: Implemented Current-Starved Ring Oscillator VCO

The sizes for the designed VCO transistors are the following:

Table 6.1: Implemented CSRO VCO transistor sizes

Transistor	Transistor Type	W(μm)	L(nm)	Number of Fingers
M1	PMOS	2.7	240	4
M2	PMOS	0.9	120	4
M9	NMOS	0.9	240	4
M3, M4, M5	PMOS	4.185	240	4
M13, M14, M15	NMOS	1.395	240	4
M6, M7, M8	PMOS	2.7	120	5
M10, M11, M12	NMOS	0.9	120	5

By testing the VCO, it is possible to show the gain curve K_{VCO} and calculate its slope. Also, a consumption curve according to its control voltage is shown.



a Current-Starved Ring Oscillator KVCO b Current-Starved Ring Oscillator Current Consumption

Figure 6.3: Implemented Current-Starved Ring Oscillator VCO Frequency Range and Current Consumption

By analyzing the given curve in Figure 6.3a, it can be concluded that the by analysing the K_{VCO} curve between 0.2V and 0.35V, VCO has the following gain:

$$K_{VCO} = \frac{\partial F}{\partial V} \approx 2.4G\left[\frac{Hz}{V}\right]. \tag{6.4}$$

Also, it can be confirmed that the VCO consumption ranges from 300µW to approximately 660µW, depending on the oscillation frequency.

The VCO phase noise can also be simulated, and the results for 1M and 10M are shown in the Figure 6.4.

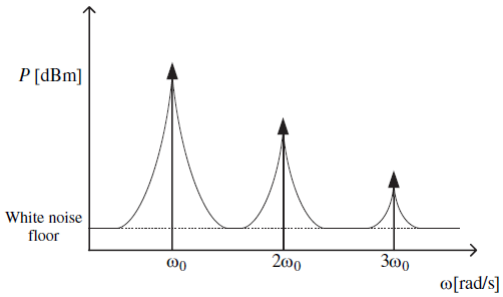


Figure 6.4: Implemented Current-Starved Ring Oscillator VCO Phase Noise

At 1MHz the VCO has $-87.73dBc/Hz$ and at 10MHz presents a $-110.4dBc/Hz$.

A table with the VCO characteristic is shown:

Table 6.2: VCO Characteristics

Frequency Range (GHz)	Gain (MHz/V)	Current (mA)	Power Consumption (mW)	Phase Noise @1MHz (dBc/Hz)	Phase Noise @ 10MHz (dBc/Hz)
0.4 - 1.5	≈ 3000	0.25 - 0.55	0.3 - 0.66	-87.73	-110.4

The following Figure 6.5 shows the Layout of the VCO block:

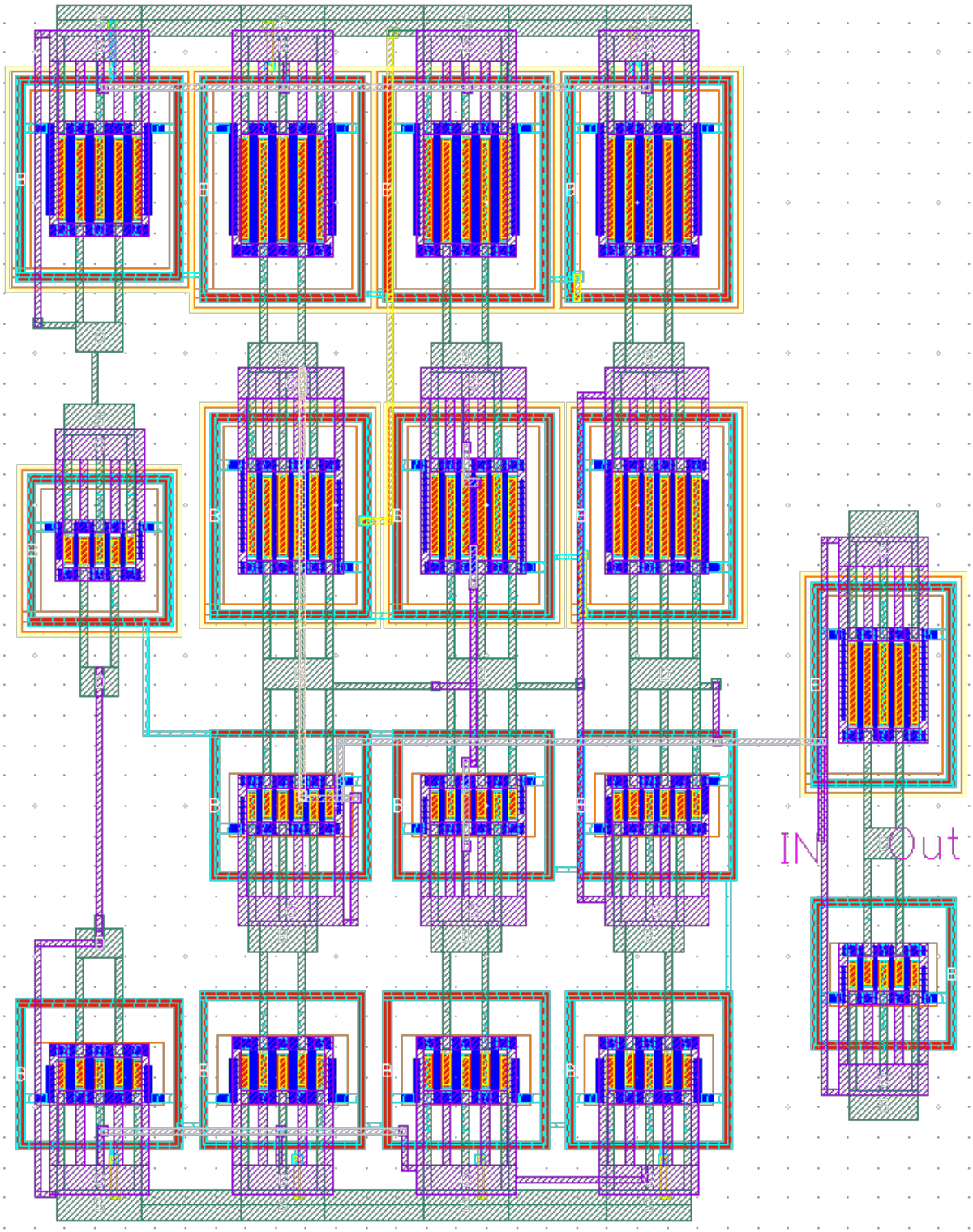


Figure 6.5: Implemented VCO Layout

6.2 Implemented Divider

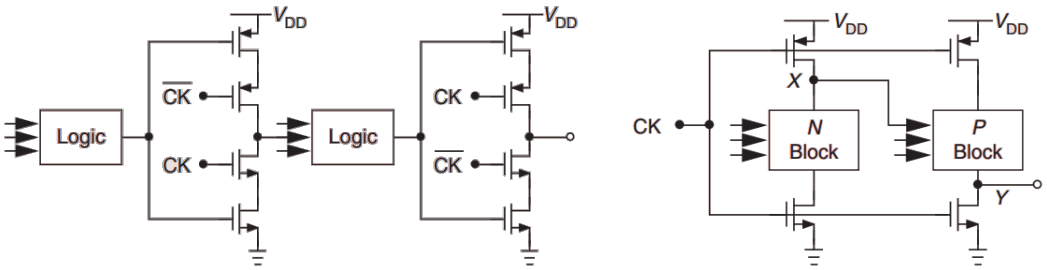
The divider chosen to be implemented in this thesis is divide-by 64 constituted by a cascade of 6 simple digital dividers presented in 5.2.2 where the chosen architecture for the Flip-Flop D is based on TSPC logic and was modified in order not to consume more current than needed, therefore ignoring the Q output of the circuit.

6.2.1 TSPC Logic

The TSPC, True Single Phase Clocked logic is widely used in high speed and low power applications.

6.2.1.1 Historical Background

The introduction of TSPC took an important role in CMOS design. In the early decade of 1980, the main issues were related to clock distribution in complex chips, heavy capacitive loading and longer interconnections that caused both slow transitions and skew, making a challenge to distribute multiple high-speed clock phases. On the other hand, it has been recognized that dynamic logic afforded simpler, faster circuits that also occupied less area than the previous type of design. Clocked CMOS logic introduced one decade before TSPC had replaced complex latches by four-transistor dynamic implementation. However, it required two non-overlapping clock phases, making the circuit deal with skew and loss of timing due to non-overlapping intervals, therefore making single-phase clocking a better approach. An example can be seen in 6.6a



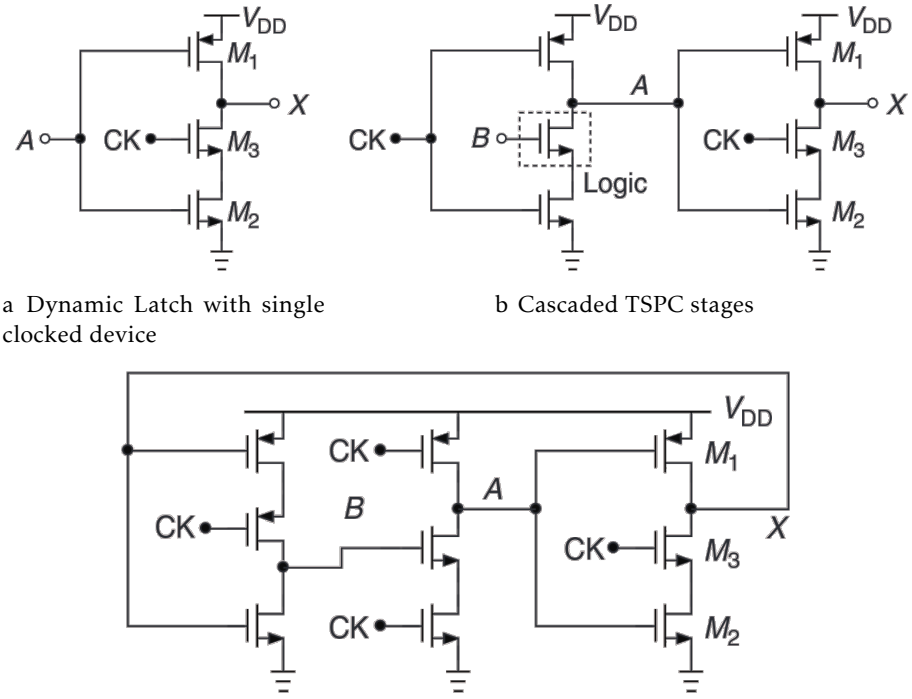
a C^2MOS Logic

b Example of single-phase clocking

Figure 6.6: C^2MOS Logic and Single-Phase Clocking Logic [22]

The previous figure, Figure 6.7 depicts a single-phase approach. Merged with the dynamic latches, the logic is made by NMOS or PMOS devices in alternate stages (NMOS and PMOS blocks, respectively). Here, when the clock (CK) is low, node X is precharged to VDD, and when CK goes high, the N block is enabled and, according to the inputs, keeps the logic value 1 or discharges it to 0. The main issue here is that the second stage begins to evaluate while the first precharges X node, a race condition that can lead to a partially charged level at Y node and hence an indeterminate logical value. This issue can

be resolved by delaying the second stage's clock or by placing an inverter at the output of each stage.



a Dynamic Latch with single clocked device

b Cascaded TSPC stages

c A three-stage master-slave flip-flop operating as a frequency divider

Figure 6.7: True Single-Phase Clocking Logic [22]

If the figure depicted in the previous Figure 6.7a is taken in account, when CK is high, the latch is reduced to an inverter. When CK is low, the circuit is in the store mode and retains the output state if node A does not change or has only a low-to-high transition. If this structure is used with a Domino stage that incorporates N-type logic, as shown in Figure 6.7b, it is known that, when CK goes low to precharge the first stage, the second stage's output remains the same. In sum, when CK is high, the first stage evaluates while the second senses, and when CK is low, the first stage is reset while the second stores. As an application example, TSPC can be used in a divide-by-two circuit. Since the cascade shown in Figure 6.7b does not invert, it is preceded with a third TSPC stage using clocked PMOS transistor Figure 6.7c and connect the output to the input. This arrangement exhibits no charge sharing [4].

6.2.2 Divider Implementation

The implemented divider is a D Flip-Flop, as depicted in 6.7c. To make a divide-by-64 divider, six of those Flip-Flops must be connected in series, as show in Figure 6.8:

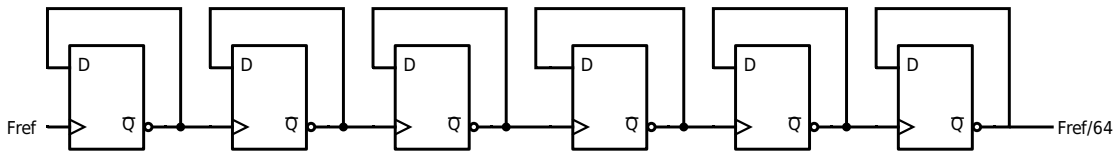


Figure 6.8: Chosen Frequency Divider

The designed D Flip-Flop for this divider has the following components and its sizes, as shown in Figure 6.9 and Table 6.3

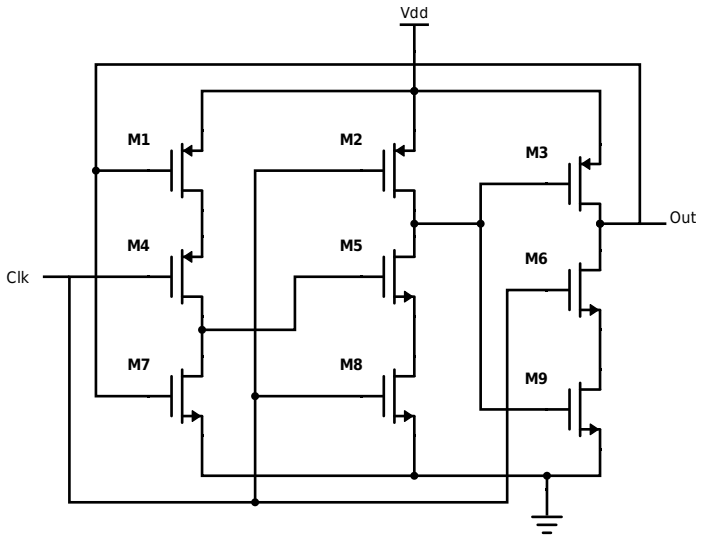


Figure 6.9: Chosen DFF

Table 6.3: D Flip-Flop Transistor Sizes for the Divider

Transistor	Transistor Type	W(µm)	L(nm)	Number of Fingers
M1, M2, M3, M4	PMOS	2.7	120	4
M5, M6, M7, M8, M9	NMOS	0.9	120	4

The designed divider was tested and the results can be seen in 6.10. Taking "Fref"as reference frequency at 1.5GHz (VCO's maximum output frequency), it can clearly be seen that the cascade of dividers works as expected, each stage divides its input frequency by two, making a total division by 64.

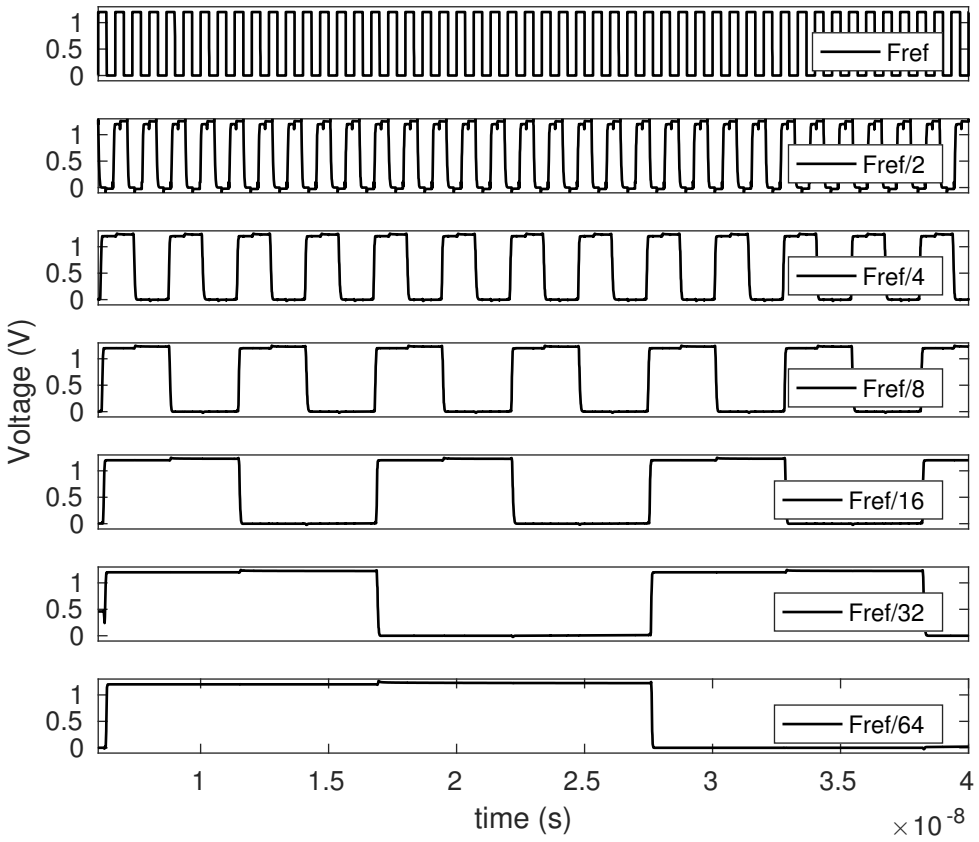


Figure 6.10: Divider Input and Output Signals

The following Figure 6.11 shows the Layout of the divide-by-64 block:

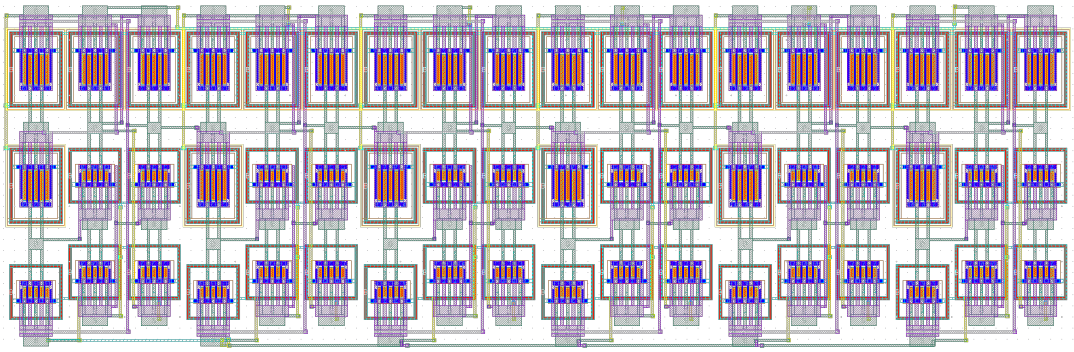


Figure 6.11: Implemented Divide-by-64 Layout

6.3 Implemented Phase-Frequency Detector and Charge Pump

6.3.1 Phase-Frequency Detector

The phase detector employed for this thesis is the classical Phase-Frequency Detector depicted in Figure 5.10c. In order to lower its consumption, a TSPC architecture for the D Flip-Flop was used. It was adapted so it can be reset and have the Q output. The following Figure 6.12 shows the circuit for the D Flip-Flop implemented.

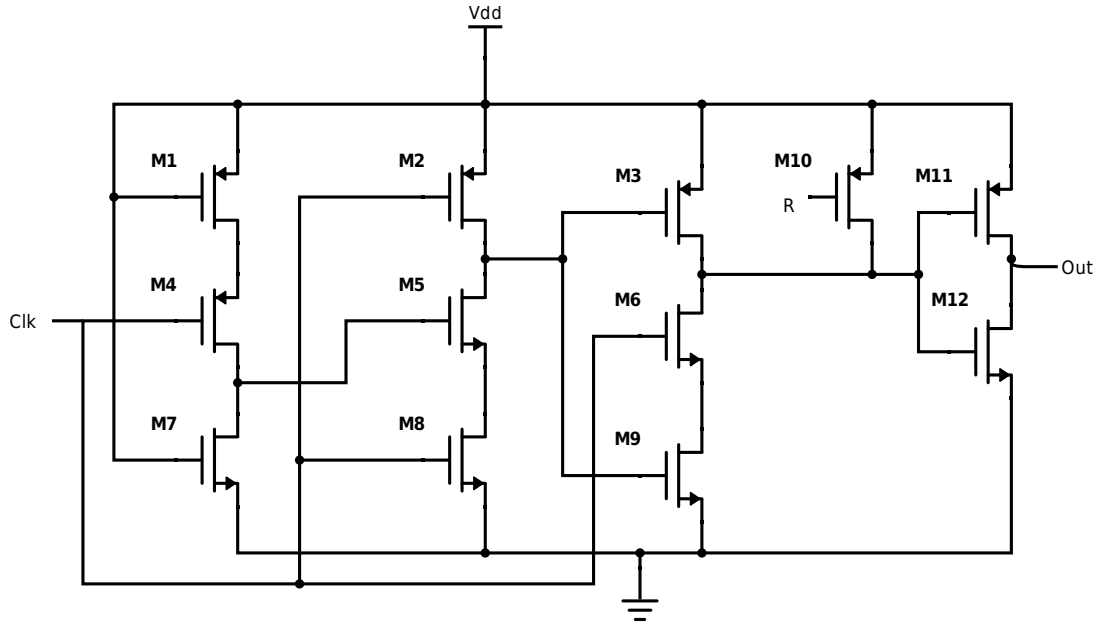


Figure 6.12: D Flip-Flop for the Implemented Phase-Frequency Detector

Table 6.4: D Flip-Flop for the Implemented Phase-Frequency Detector Transistor Sizes

Transistor	Transistor Type	W(μm)	L(nm)	Number of Fingers
M1, M2, M3, M4	PMOS	2.7	120	4
M5, M6, M7, M8, M9	NMOS	0.9	120	4
M10	PMOS	2.7	360	2
M11	PMOS	2.7	120	4
M12	NMOS	0.9	120	4

Noting that reset of this Flip-Flop is constituted by a PMOS transistor, it is known that it must be activated at a logical value of "1". For this, instead of a AND gate between the path of Up and Down signals and the Reset path, a NAND gate is implemented, reducing its power consumption and area by not implementing an inverter.

The NAND gate is depicted in the following Figure 6.13:

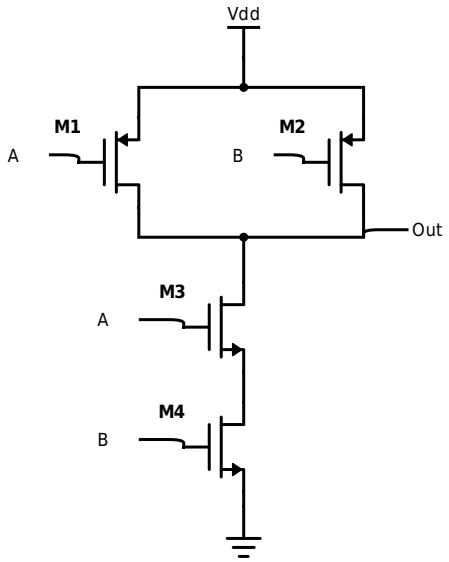


Figure 6.13: NAND gate

Table 6.5: NAND gate transistor sizes

Transistor	Transistor Type	W(µm)	L(nm)	Number of Fingers
M1, M2	PMOS	2.7	360	4
M3, M4	NMOS	0.9	360	4

The following Figure 6.14 shows the Layout of the phase-frequency detector block:

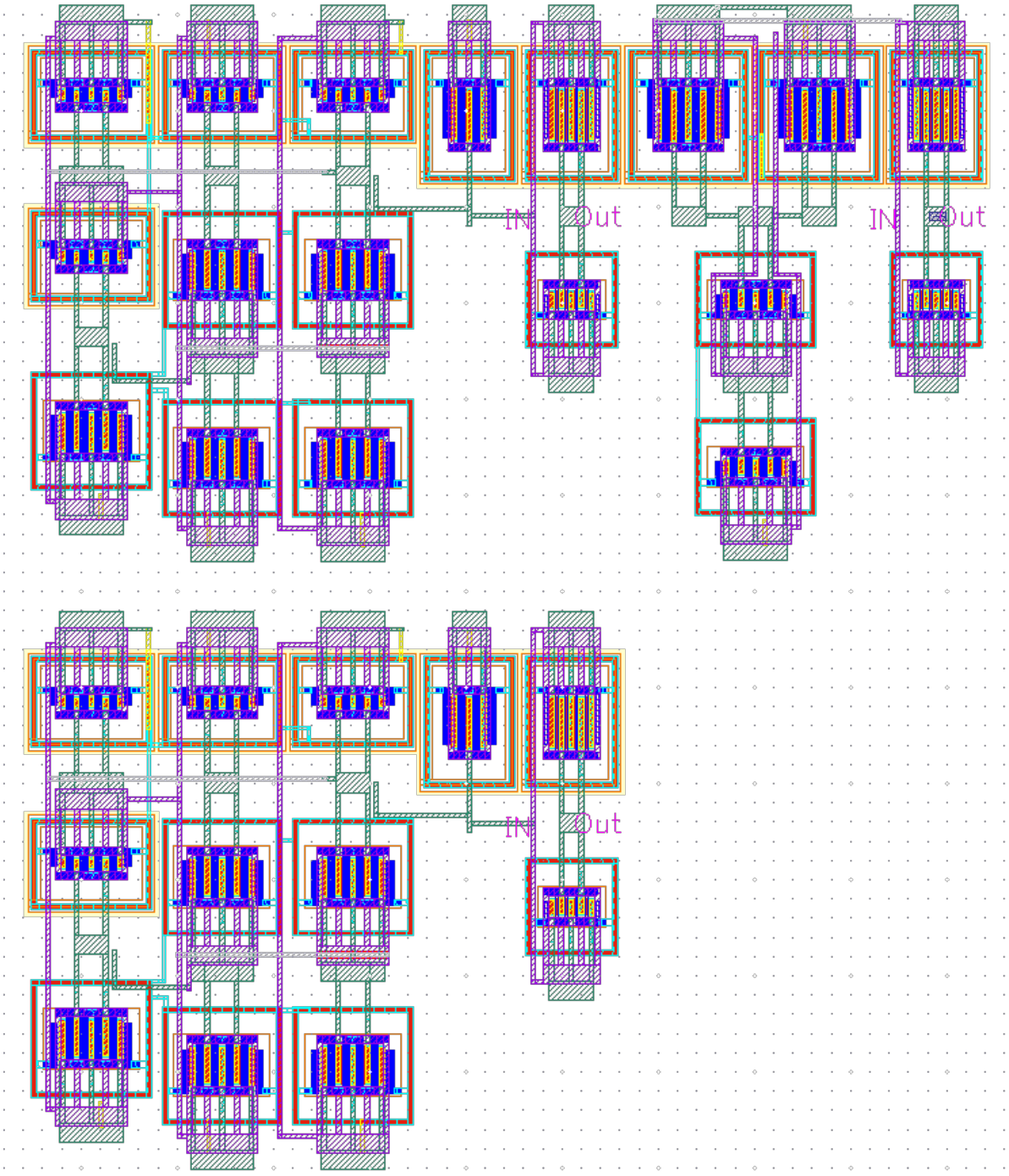


Figure 6.14: Implemented Phase-Frequency Detector Layout

6.3.2 Charge Pump

The charge-pump designed takes into account the area and the power consumption, therefore it is one the most simple charge pumps. It is constituted by 6 transistors and a resistor, as it can be seen in the following Figure 6.15.

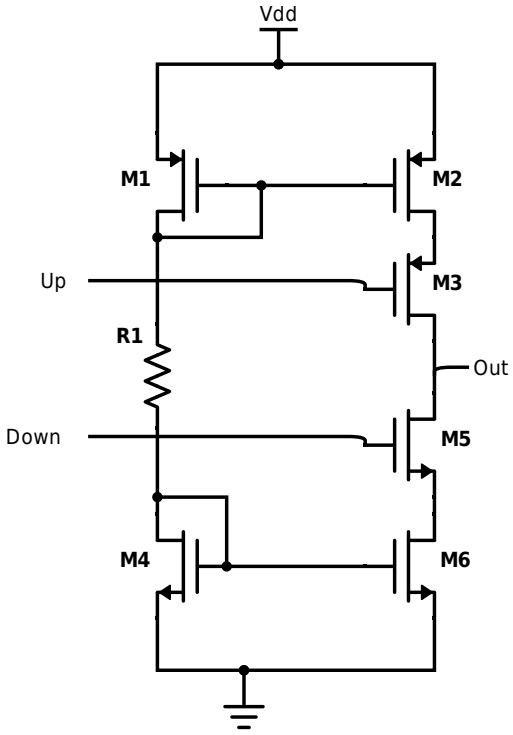


Figure 6.15: Charge Pump

Table 6.6: Charge Pump Component Sizing

Component	Type	W(µm)	L(nm)	Number of Fingers	Value (Ohm)
M1, M2, M3	PMOS	2.7	360	4	-
M4, M5, M6	NMOS	0.9	360	4	-
R1	Resistor	-	-	-	25k

The following Figure 6.16 shows the Layout of the phase-frequency detector block:

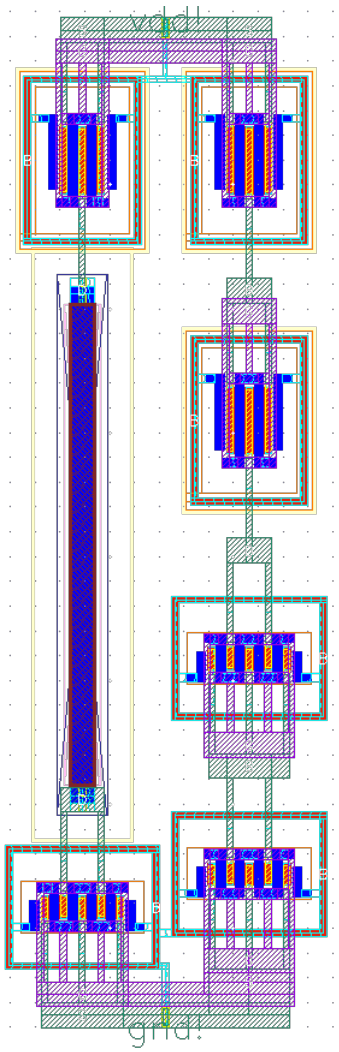


Figure 6.16: Implemented Charge Pump Layout

6.4 Implemented Loop Filter

In this work the loop filter is a second order low-pass filter. It converts the charge pump current into a control voltage after filtering high frequency signal components and suppressing the noise and stabilizing the loop [26].

The topology of the filter used is shown in Figure 6.17. R_1 provides a stabilizing zero, improving the phase margin hence improving the PLL transient response. C_2 is needed to suppress the ripples (with a value of $I_{CP}.R_1$) on the control voltage caused by R_1. To avoid under damped settling C_2 must be about ten to twenty times smaller than C_1 [22] [26].

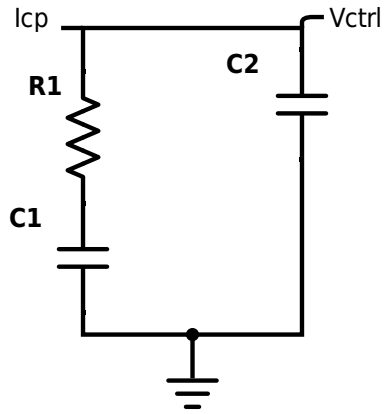


Figure 6.17: Second order low-pass filter

Table 6.7: Second Order Low-pass Filter component values

Component	Type	Value
R1	Resistor	1k Ohm
C1	Capacitor	20pF
C2	Capacitor	4pF

The correspondent transfer function can be obtain using linear analysis and is given by:

$$F(s) = \frac{V_{ctrl}(s)}{I_{cp}(s)} = Z_{eq}(s) \tag{6.5}$$

and $Z_{eq}(s)$ is

$$Z_{eq}(s) = \frac{s + \frac{1}{R_1 C_1}}{sC_2\left[s + \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}}\right]} \tag{6.6}$$

According to the transfer function 6.6, it can be possible to identify one zero and two poles, being these, in order:

$$Z_1 = -\frac{1}{R_1 C_1} \tag{6.7}$$

$$P_1 = -\frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \tag{6.8}$$

$$P_2 = 0 \tag{6.9}$$

The Figure 6.18 shows the Bode plot of the designed loop filter:

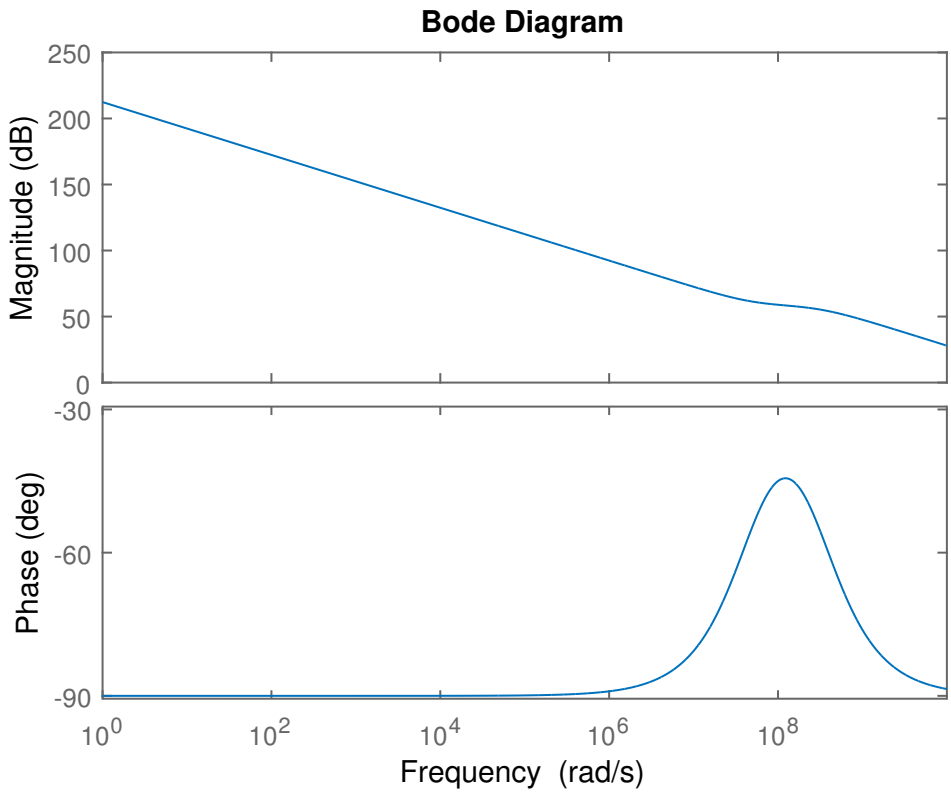


Figure 6.18: Loop Filter Bode Plot

Through the analysis of the loop filter transfer function and graph of the Bode plot, it can be concluded that it has a zero on 7.96MHz, a pole in the origin and another in 47.75MHz. The pole on 47.75MHz marks the PLL loop bandwidth. In order for the PLL to lock, it needs a large loop bandwidth due to VCO's large gain.

Although a full PLL phase noise calculation was not possible, [4] demonstrates that the loop bandwidth clearly defines the phase noise. In its literature, it is shown that the loop bandwidth curve will follow the VCO phase noise curve.

6.5 PLL simulation

In the following Figures, it is possible to see the PLL locking time, the phase difference between the reference signal and the divider signal and the resulting control voltage V_{ctrl}.

The first case is depicted for a 16MHz reference:

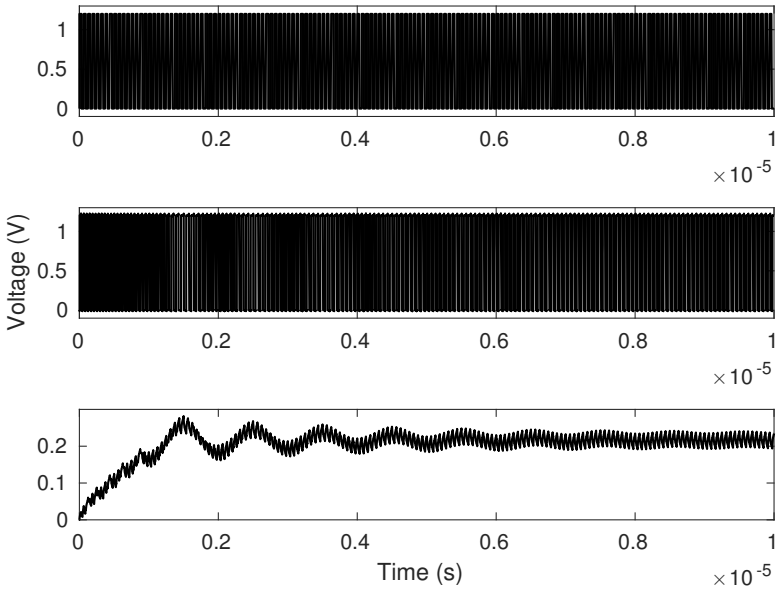


Figure 6.19: Final Results

By analyzing the Figure 6.19, it is possible to see that the PLL presents a lock time of approximately 1µs. To analyze the previous figure with more detail, a zoomed version is depicted in the following Figure 6.20.

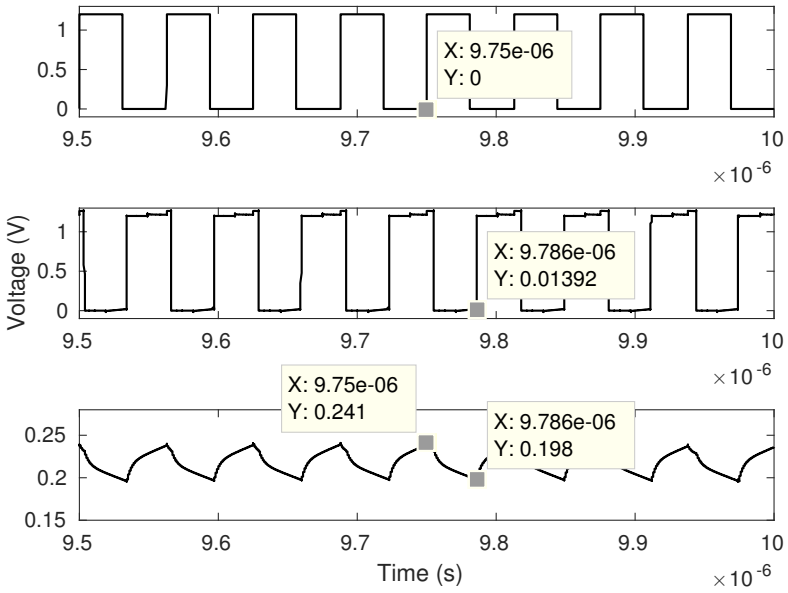


Figure 6.20: Final Results Zoom

As it can be seen through the analysis of the Figure 6.20, the divider waveform has a 36nS delay, resulting in a 41.7mV of ripple when the PLL is in lock state.

A second simulation is made for 8MHz reference signal:

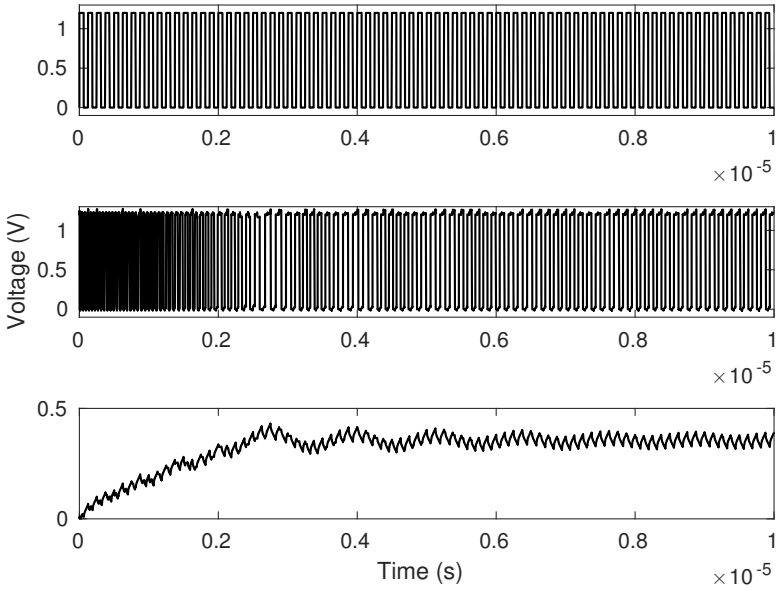


Figure 6.21: Final Results

By analyzing the Figure 6.21, it is possible to see that the PLL presents a lock time of approximately 2µs. It is possible to conclude that by lowering the reference frequency by a factor of two, the locking time enlarges by two.

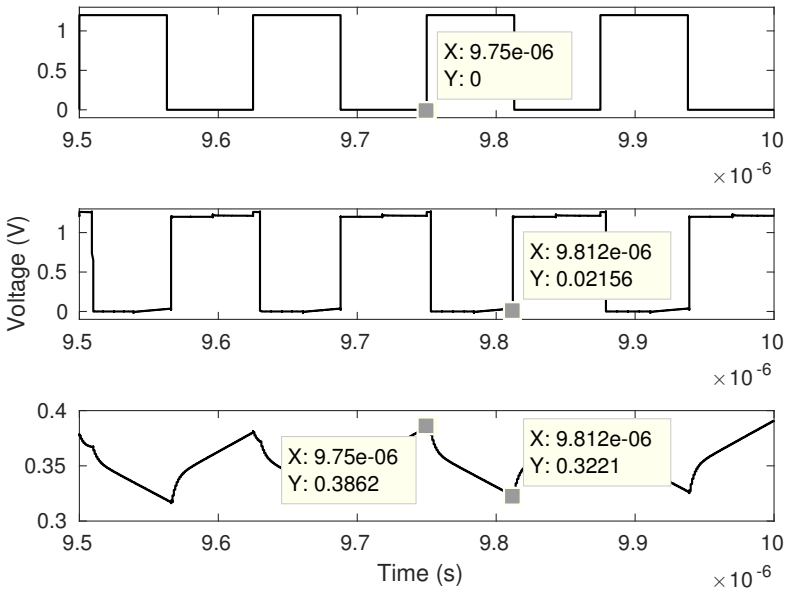


Figure 6.22: Final Results Zoom

As it can be seen through the analysis of the Figure 6.22, the divider waveform presented has a 62nS delay, resulting in a 76.5mV of ripple when the PLL is in lock state.

Comparing both simulations, it is possible to state that the PLL is capable of locking on a reference frequency range from 8MHz to at least 16MHZ.

In the Figure 6.23 the layout of the full PLL is shown:

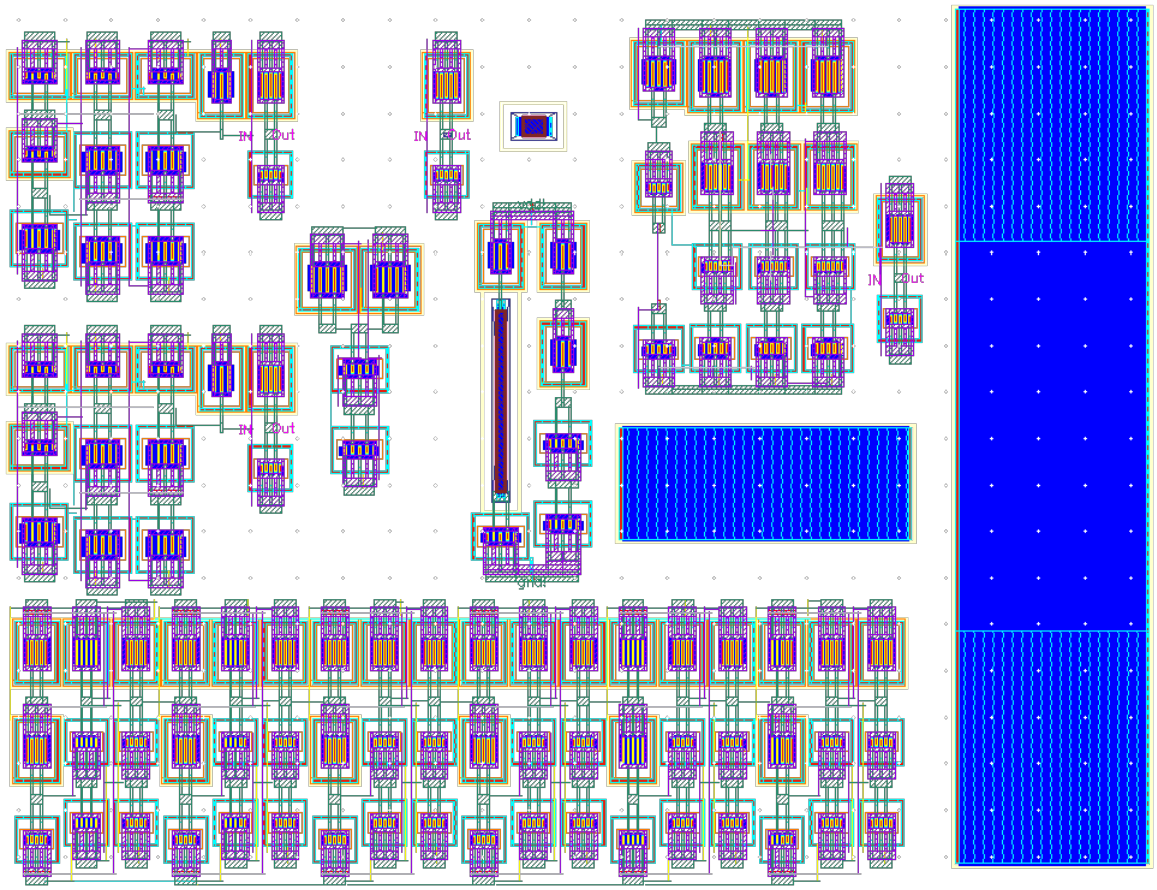


Figure 6.23: Full PLL Layout

CHAPTER 7

Conclusions and Future Work

The thesis presented offers a solution to the problem proposed: designing a low power PLL in advanced 130nm CMOS technology for ISM applications. The concept of the main blocks was introduced, studied and the best solution for low power not compromising performance and the occupied area was implemented. This compromise was taken in order to fulfill all the specifications.

Beginning with the VCO block, a simple three stage Current-Starved Ring Oscillator was used, with minimum sizing possible and least consumed current. The next block, called the frequency divider is composed by six TSPC D Flip-Flop stacked. The same philosophy for the sizing and power consumption was applied as before. The Phase-Frequency Detector was also composed by two modified TSPC D Flip-Flop, a NAND Gate, an inverter and a Charge pump all with minimum sizing, not compromising performance. Finally, the loop filter composed by a resistor and two capacitors was designed in order to stabilize the system.

The main specifications were met, and a table of comparison will be presented:

Table 7.1: PLL Design Specifications and Implemented Solution

	Proposed Specifications	Implemented Specifications
Input Reference Clock Frequency	16 MHz	16 MHz
VCO Output Frequency Range	500MHz - 1.5GHz	400MHz - 1.5GHz
PLL Output Frequency	1GHz	1GHz
Power Consumption	<2 mW	1.3mW

7.1 State of the art

In this chapter a table of comparison between the designed PLL and other works will be provided it is used to take some conclusions about this thesis.

Table 7.2: PLL Comparison

	This Work	[29]	[25]	[8]	[9]	**Other Work - Pedro Mateus**
VCO Type	CSRO	Diff RO	LC	Diff RO	Diff RO	CSRO
Supply Voltage [V]	1.2	3.3	1.8	1.8	1.8	0.8
VCO Gain K_{vco} [GHz/V]	≈ 3	-	-	1.8	1.72	> 10
VCO Tuning Range [GHz]	0.4 -1.5	0.1 - 0.56	1.47 - 1.83	0.5 - 1.1	0.32 - 0.96	1 - 6
PLL/VCO Output [GHz]	1	0.35	1.65	0.8	0.915	1 - 6
VCO Power Consumption [mW]	0.3 - 0.66	12	-	-	-	0.0995 - 0.5753
PLL Power Consumption [mW]	1.3	-	11.2	25.15	20	212.78 - 922.4
VCO Phase Noise @ 1MHz Offset [dBc/Hz]	-87.73	-	-118	-	-93.03	-78.5
Size [µm]	123.9 x 95	410 x 210	0.53 [mm^2]	290 x 160	540 x 450	218 x 347
Technology [nm]	130	350	180	180	180	65

Comparing with other works it can be concluded that with newer technology it is possible to achieve higher oscillation frequency but with lower power consumption and occupied area. Also, it is possible to see that the designed PLL has the lowest area of all the other works. The designed VCO has a considerably high gain, hence a high tuning range and the lowest power consumption comparing with all the works except for the one with 65nm. The phase noise is slightly lower than other works due to the use of single-ended VCO; it is known that with the use of differential outputs implies a higher noise immunity, which lowers phase noise.

7.2 Future Work

In a possible future work, a full-quadrature PLL with better performance could be implemented in order to be a part of a modern transceiver, architecture which is composed by several quadrature outputs. Also, another type of PLL such as a All-Digital PLL could be implemented due to its many applications.

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